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IQE plc

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

IQE plc,

Plaintiff,

v.

NEWPORT FAB, LLC d/b/a JAZZ SEMICONDUCTOR, TOWER U.S. HOLDINGS INC., TOWER SEMICONDUCTOR LTD., PAUL D. HURWITZ, EDWARD PREISLER, DAVID J. HOWARD, and MARCO RACANELLI,

Defendants.

CASE NO. 8:22-cv-00867

COMPLAINT FOR:

(1) VIOLATION OF DEFEND TRADE SECRETS ACT

(2) VIOLATION OF CALIFORNIA UNIFORM TRADE SECRETS ACT

(3) CORRECTION OF INVENTORSHIP

(4) BREACH OF CONTRACT

(5) VIOLATION OF CALIFORNIA UNFAIR COMPETITION ACT

(6) INTENTIONAL INTERFERENCE WITH PROSPECTIVE ECONOMIC ADVANTAGE

(7) NEGLIGENT INTERFERENCE WITH PROSPECTIVE ECONOMIC ADVANTAGE

DEMAND FOR JURY TRIAL

Plaintiff IQE plc (IQE), for its complaints against Newport Fab, LLC, Tower U.S. Holdings Inc., Tower Semiconductor Ltd., Paul D. Hurwitz, Edward Preisler, David J. Howard, and Marco Racanelli (collectively, "Tower"), alleges as follows:

NATURE OF THIS ACTION

1. This is an action for claims of misappropriation of IQE's trade secrets under both the Federal Defend Trade Secrets Act and the California Uniform Trade Secrets Act over Tower's unauthorized use of trade secrets covered by a mutually binding non-disclosure agreement (NDA) between IQE and Tower (Exhibit 1).

2. This action also encompasses a claim for correction of inventorship, under 35 U.S.C. § 256, of U.S. Patent Nos. 11,164,740 (the '740 patent) (Exhibit 2), 11,195,920 (the '920 patent) (Exhibit 3), 11,145,572 (the '572 patent) (Exhibit 4), and U.S. Patent Application 17/400,712 (the '712 application) (Exhibit 5), stemming from theft of IQE's inventions and trade secrets, which formed the basis for the claimed technology.

3. IQE also seeks relief for breach of contract under the aforementioned NDA.

4. IQE brings a claim of unfair competition under the Unfair Competition Law of California. C.A. Bus. & Prof. Code § 17200.

5. Finally, this action also brings a claim for intentional interference with prospective economic advantage, as well as a claim of negligent interference with economic advantage, because Tower's disclosure of IQE's trade secrets in Tower's patents and application wrongfully damaged IQE's relationships with potential customers and market position. *See* 28 U.S.C. § 167; *see also* Cal. Civ. Code § 3426.

PARTIES

6. IQE plc is a British corporation that has its head office at Pascal Close, St Mellons, Cardiff, CF3 0LW, UK, where it was also incorporated. IQE plc

operates several U.S. manufacturing sites directly or indirectly through its subsidiaries.

7. On information and belief, Newport Fab, LLC is a corporation organized under the laws of Delaware with its principal place of business at 4321 Jamboree Road, Newport Beach, California. In 2019, Newport Fab, LLC did business under the names "Jazz Semiconductor" and "TowerJazz."

8. On information and belief, Newport Fab, LLC, is indirectly held by Tower Semiconductor Newport Beach, Inc., itself indirectly held by Tower Semiconductor NPB Holdings, Inc. Both of these holding companies are organized under the laws of Delaware and share the office at 4321 Jamboree Road, Newport Beach, California, 92660 with Newport Fab, LLC.

9. On information and belief, these companies are themselves held directly and are controlled by Tower U.S. Holdings Inc., a corporation organized under the laws of Delaware. Tower U.S. Holdings Inc. thus acts in this forum through its subsidiaries and holdings. It is the agent of service for Tower Semiconductor Ltd., and its principal office is 2570 North First Street, Suite 480 San Jose, California, 95131.

10. On information and belief, Tower Semiconductor Ltd. is the parent company that directly holds Tower U.S. Holdings Inc. and controls and directs Newport Fab, LLC. Tower Semiconductor Ltd. thus acts in this forum through its subsidiaries and holdings. Tower Semiconductor Ltd. is an Israeli company with its head offices in the Ramat Gavriel Industrial Park, Shaul Amor Street, Post Office Box 619, Migdal Haemek, 2310502 Israel.

11. On information and belief, Paul D. Hurwitz was a former director of technology development at Newport Fab, LLC during the relevant period in 2018-2020. He currently works as the Director of Foundry Engineering at Rockley Photonics Inc. He is domiciled in Irvine, California.

12. On information and belief, Edward Preisler is a current director of technology development at Newport Fab, LLC, and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in San Clemente, California.

13. On information and belief, Dr. David J. Howard is an executive director and fellow of Tower Semiconductor Ltd. and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in Newport Beach, California.

14. On information and belief, Marco Racanelli is the senior vice president and general manager of Newport Fab, LLC, and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in Santa Ana, California.

JURISDICTION AND VENUE

15. This is a civil action seeking damages, injunctive relief, and other equitable relief under an action for correction of inventorship, 35 U.S.C. § 256, the Defend Trade Secrets Act, 18 U.S.C. § 1836, and California statutory and common law.

16. This Court has subject matter jurisdiction over this case pursuant to 28 U.S.C. § 1331 and 18 U.S.C. § 1836(c), as it involves actions arising under the laws of the United States. This Court has supplemental jurisdiction over the state law claims under 28 U.S.C. §1367, as they are so related to the federal claims as to form a single case.

17. Tower resides within the Central District of California and is subject to personal jurisdiction in the State of California because the unlawful conduct occurred in, and causes injuries in, California and this district specifically and because Tower (a) has signed an NDA that specifies the law and venue of California as the proper jurisdiction, (b) has directed their activities concerning IQE, including the misappropriation of IQE's trade secrets, in California and this

district, (c) transacts business in California, including operating a branch corporation in this district, (d) enters into contracts and partnerships with individuals and entities in this district, and (e) offers products and services for sale in this district.

18. Venue is proper in this district pursuant to 28 U.S.C. § 1391(b) because this is a district in which a substantial portion of the events giving rise to the claims occurred and in which IQE's injuries were suffered, as set forth below.

BACKGROUND

19. Since its founding in 1988, IQE has been the leading innovator and supplier of advanced wafer products, which are central to a broad range of downstream technologies, such as semiconductor devices, transistors (e.g., high electron mobility transistors (HEMTs), BiHEMTs, pseudomorphic high electron mobility transistors (pHEMTs), heterojunction bipolar transistors (HBTs), and bipolar field-effect transistors (BiFETs)), passive components, complementary metal-oxide-semiconductor (CMOS) processing, photonic devices, wireless devices, and radio frequency (RF) devices (e.g., RF switches and RF filters).

20. IQE's business model is unique in the industry, as IQE possesses processes to develop custom, individualized solutions to meet its customers' needs. These processes are a closely guarded trade secret, which has granted IQE a dominant position as a market innovator. IQE's unique capabilities were what drew Tower to pursue an exclusive licensing deal with IQE relating to IQE's porous silicon and epitaxial technologies.

21. IQE is the world's leading advanced wafer manufacturer and supplier and is the largest pure-play compound semiconductor wafer supplier with capability for volume manufacture across all semiconductor materials, including chemical vapor deposition (CVD), molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) reactors for a variety of custom semiconductors.

22. IQE specializes in, among other applications, advanced Group IV and compound Group III-V semiconductors (e.g., silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), gallium antimonide (GaSb), indium antimonide (InSb), and multi-element alloys), including porous semiconductors. IQE also specializes in advanced semiconductor wafers utilized in wireless and RF products, such as transistors and switches, including epitaxy on porous silicon wafers as an alternative to silicon-on-insulator (SOI)-based devices. IQE's custom porous epitaxial wafers can be used for advanced microelectronics, optoelectronics, photonics, sensing, and high-performance RF and radiation-sensitive applications.

23. Tower is another figure in the semiconductor industry, known for the creation of specialized integrated circuits that are fabricated using wafers of the kind that IQE makes.

A. IQE's Business Model and Proprietary Information

24. IQE plc is a British semiconductor company founded in 1988; it also operates in the United States through subsidiaries in Pennsylvania, Massachusetts, North Carolina, and Washington.

25. Since its founding, IQE has been an industry leader in the manufacture of advanced epitaxial wafers and materials technologies used in a broad range of downstream technologies. In addition to manufacturing ready-made wafers, IQE also creates customized semiconductor solutions to meet its customers' specific needs. It is a one-stop-shop for the advanced Group IV and compound Group III-V semiconductor wafer needs of the world's leading semiconductor manufacturers.

26. To maintain its market position as a leader and innovator on a number of fronts, IQE protects a range of intellectual property pertaining both to the individual products it produces and sells and also the methods by which it develops semiconductor solutions—including RF solutions. While IQE obtains patents on certain products and technologies, many of the processes that are crucial to its

competitive advantage are kept as trade secrets. This is due to the difficulty in policing patents to processes and due to IQE's business model of contracting with customers for custom product solutions.

27. IQE's porous silicon technology is a superior alternative to high-resistivity silicon-on-insulator (SOI) substrates with a trap-rich layer. Porous silicon can achieve high-resistivity properties on a standard silicon CMOS wafer, rather than an SOI wafer. IQE's porous silicon technology produces comparable or better device performance than the previous SOI technology, is a simpler manufacturing process and has the additional advantage of using only a standard low-resistivity silicon CMOS substrate rather than a high-resistivity SOI substrate. Further, porous silicon can be thick enough to fully trap fringing fields, which significantly improves performance of devices fabricated on the porous silicon structure.

28. In 2018, based on these innovations, IQE began developing additional applications and products using its innovative porous silicon technology, which had the ability to outperform the competition. One such potential application that looked particularly promising was developing a high-performance RF switch using IQE's porous silicon technology. Another promising potential application was developing localized patterned porous segments, with adjacent porous and non-porous segments, combining IQE's porous silicon technology with RF switch technology.

B. Past Business Relations

29. On November 12, 2015, IQE and Tower entered into a mutually binding Non-Disclosure Agreement (NDA) as to any confidential information they disclose to one another as part of their business transactions. That NDA is attached as Exhibit 1 to this Complaint and is incorporated by reference. The NDA protects "all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the disclosing party to the receiving

party, as well as all information in tangible form that bears a 'confidential,' 'proprietary,' 'secret,' or similar legend and discussions of that information relating to that information whether those discussions occur prior to, concurrent with, or following the disclosure of the information." Exhibit 1. The NDA also specifies the proper venue and law for any dispute "[t]his agreement, as well as any disputes arising out of or relating to this agreement, shall be interpreted under and governed by the laws of the State of California. Any disputes arising out of or relating to this Agreement and not resolved by the parties themselves shall be commenced solely in the Federal or state courts located within the State of California. In such event, each party irrevocably agrees to submit to the personal jurisdiction of such courts and waives any objection to such venue." *Id.*

C. IQE Approaches Tower about a Potential Collaboration

30. In November 2018, IQE and Tower began discussing a potential collaboration providing IQE's porous silicon technology with Tower's RF sensor technology to create new semiconductor products.

31. As a part of the parties' mutual exploration of a potential collaboration, Tower requested, and IQE provided, proprietary trade secrets pertaining to IQE's porous silicon and crystalline epitaxy wafers. For example, on November 6, 2018, IQE presented its epitaxy on porous silicon technology to Tower, followed by sending a copy of the presentation given with additional information and background papers. And, on July 24, 2019, IQE presented its epitaxy on porous silicon technology for RF switches to Tower, followed by sending a copy of the presentation given. Copies of these presentations are attached as Confidential Exhibits 6 and 7, respectively, and are incorporated by reference. Formal presentations were not the only times IQE shared information on their trade secrets as they also furnished Tower with emails answering specific questions about IQE's capabilities, technical papers, and experimental data. *See* Confidential Exhibit 8, 9.

32. All of these meetings and presentations, and the information exchanged therein, were protected by the mutually binding NDA signed by the parties in November 2015. Because the information at issue contained IQE's highly valuable and important trade secrets, IQE took additional steps prior to these meetings to remind Tower of its ongoing obligation under that NDA not to use or disclose any information conveyed without IQE's consent. This obligation included "all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the disclosing party to the receiving party, as well as all information in tangible form that bears a 'confidential,' 'proprietary,' 'secret,' or similar legend and discussions of that information relating to that information whether those discussions occur prior to, concurrent with, or following the disclosure of the information." Exhibit 1. All slides that IQE representatives displayed during these meetings and presentations were clearly marked as containing highly confidential information proprietary to IQE. *See* Confidential Exhibit 6, 7.

33. Due to IQE's innovative processes and technology, Tower displayed a strong interest in IQE's porous silicon technology and proposed a contract for a multi-year supply agreement. One of the terms of Tower's proposed Memorandum of Understanding ("MOU") was a multi-year period of exclusivity, during which IQE could not supply any other customer with its porous silicon technology solutions. This MOU is attached to this complaint and incorporated by reference as Confidential Exhibit 11. *See also* Confidential Exhibit 10.

34. IQE was not willing to forego selling one of its flagship innovations to other customers, and it counter-offered that it would enter into a non-exclusive partnership with Tower with a preferential pricing scheme.

35. This led to an impasse in negotiations as Tower insisted in an email on October 21, 2019, that exclusivity would need to exist in order for any deal to go forward. A true copy of this email is attached as Confidential Exhibit 10 and is incorporated by reference.

36. Ultimately, Tower's strong desire to exclusively practice IQE's proprietary technology, and the failure to align on a mutually acceptable preferential pricing scheme, caused a breakdown in negotiations. On February 24, 2020, IQE and Tower concluded that the planned collaboration could not go forward and agreed to end negotiations.

D. Tower Pursues Exclusive Rights to IQE's Porous Silicon Technology

37. On October 9, 2019—less than three weeks after presenting IQE with a draft memorandum of understanding that granted Tower a three-year period of exclusivity and only six weeks after IQE disclosed their invention for porous semiconductor layers for RF devices—Tower filed a patent application on "Semiconductor Structure Having Porous Semiconductor Layer for RF Devices." Tower secretly copied into their patent application IQE's trade secret information that was communicated to Tower during the parties' confidential meetings. This application would eventually be granted as the '740 patent. A copy of the '740 patent is attached as Exhibit 2 to this Complaint and is incorporated by reference.

38. The '740 patent names Paul Hurwitz, Edward Preisler, David Howard, and Marco Racanelli as inventors. *See* Exhibit 2. Each of these individuals was directly involved in the negotiations with IQE and either directly received and reviewed IQE's proprietary information during the confidential meetings or had access to it through subsequent discussions.

39. For example, Paul Hurwitz attended the confidential meeting on the scope of the proposed joint development. He defined the desired specifications for the porous silicon samples and requested follow-up information.

40. Edward Preisler participated in several confidential discussions regarding the different types of porous substrate development at IQE. David Howard also participated in the confidential discussions, was privy to confidential information, and observed the progress of the porous silicon discussion specifically.

41. Marco Racanelli was a senior vice president of Tower and oversaw much of the negotiations. Marco Racanelli gave specific directives to the other Tower employees on what to negotiate for, and at times Marco Racanelli negotiated directly with IQE. On September 13, 2019, a month before Tower began filing patents derived from IQE's intellectual property, Marco Racanelli emailed Wayne Johnson, head of wireless business development at IQE, to state that Tower had a need for IQE's porous silicon technology and were under a time pressure to make an agreement.

42. All claims of the '740 patent recite the porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '740 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations and discussions between the parties.

43. Specifically, at least claims 1-4, 8-11, 14, 15, and 17-19 of the '740 patent recite proprietary trade secrets that IQE communicated to Tower:

(a) For example, claim 1 of the '740 patent recites: "A semiconductor structure comprising: a substrate having a first dielectric constant; a porous semiconductor layer situated over said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer; said porous semiconductor layer having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 2.

(b) Claim 4 of the '740 patent recites: "The semiconductor structure of claim 1, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(c) Claim 8 of the '740 patent recites: "A semiconductor structure comprising: a porous silicon layer; at least one crystalline epitaxial layer situated directly on said porous silicon layer; first and second transistors situated in said at least one crystalline epitaxial layer; an electrical isolation region separating said first and second transistors." *Id.*

(d) Claim 9 of the '740 patent recites: "The semiconductor structure of claim 8, wherein said porous silicon layer is situated over a bulk silicon substrate." *Id.*

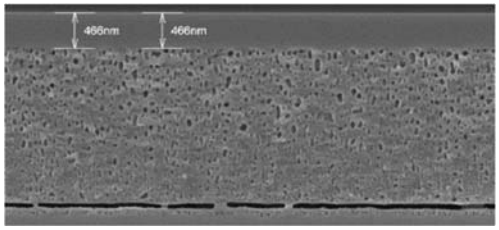
(e) Claim 11 of the '740 patent recites: "The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch." *Id.*

(f) Claim 14 of the '740 patent recites: "A semiconductor structure comprising: a porous semiconductor layer situated over a substrate, said porous semiconductor layer having a higher resistivity than said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer." *Id.*

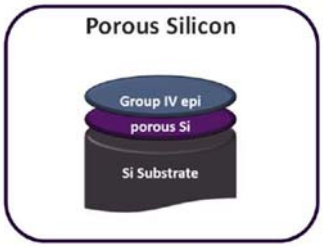
(g) Claim 15 of the '740 patent recites: "The semiconductor structure of claim 14, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material." *Id.*

(h) Claim 19 of the '740 patent recites: "The semiconductor structure of claim 14, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

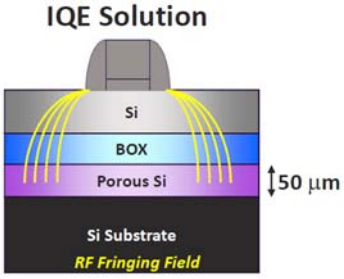
44. The form and function of the semiconductor structures contemplated by the '740 patent and recited in its claims are identical to the porous semiconductor structures that are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential presentations to Tower on November 6, 2018 ("2018 Presentation") and on July 24, 2019 ("2019 Presentation"), IQE presented examples of IQE's porous silicon technology, epitaxy on porous silicon, and applications for RF devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

substantively similar to Tower's claims in the '740 patent. Indeed, the 2019 Presentation stated "[p]orous Si for RF Switches…[s]ignificantly improved harmonics…[n]o change in device architecture." (Confidential Exhibit 7, Pg. 14.)

45. On October 10, 2019, Tower applied for a second patent—the '920 patent—naming the same inventors as the '740 patent and further misappropriating IQE's trade secrets in its claims. All claims of the '920 patent recite porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '920 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations and discussions between the parties. A copy of the '920 patent is attached as Exhibit 3 to this Complaint and is incorporated by reference.

46. Specifically, at least claims 1-6, 8-12, 14-17, and 19 of the '920 patent claim proprietary trade secrets that IQE communicated to Tower and the named inventors:

(a) For example, claim 1 of the '920 patent recites: "A semiconductor structure comprising: a porous semiconductor segment adjacent to a first region of a substrate; at least one crystalline epitaxial layer situated over said porous semiconductor segment and over said first region of said substrate; a first semiconductor device situated in said at least one crystalline epitaxial layer over said porous semiconductor segment; a second semiconductor device situated in said at least one crystalline epitaxial layer over said first region of said substrate but not over said porous semiconductor segment; said first region of said substrate having a first dielectric constant, and said porous semiconductor segment having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor segment reduces signal leakage from said first semiconductor device." *See* Exhibit 3.

(b) Claim 2 of the '920 patent recites: "The semiconductor structure of claim 1, wherein a second region of said substrate is situated under said porous semiconductor segment and under said first region of said substrate." *Id.*

(c) Claim 5 of the '920 patent recites: "The semiconductor structure of claim 1, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(d) Claim 8 of the '920 patent recites: "A semiconductor structure comprising: a porous silicon segment adjacent to a first region of a bulk silicon substrate; at least one crystalline epitaxial layer situated over said porous silicon segment and over said first region of said bulk silicon substrate; a first transistor situated in said at least one crystalline epitaxial layer over said porous silicon segment; a second transistor situated in said at least one crystalline epitaxial layer over said first region of said bulk silicon substrate but not over said porous silicon segment; an electrical isolation region separating said first and second transistors." *Id.*

(e) Claim 11 of the '920 patent recites: "The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch." *Id.*

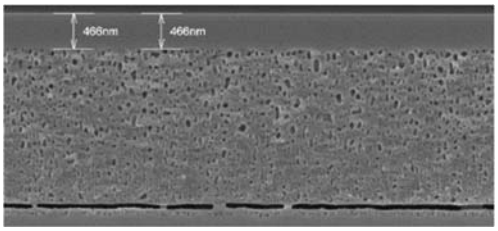
(f) Claim 14 of the '920 patent recites: "A semiconductor structure comprising: a porous silicon segment adjacent to a bulk silicon substrate; at least one crystalline epitaxial layer having a first region situated over said porous silicon segment; said at least one crystalline epitaxial layer having a second region situated over said bulk silicon substrate but not over said porous silicon segment; an electrical isolation region separating said first region of said at least one crystalline epitaxial layer from said second region of said at least one crystalline epitaxial layer." *Id.*

(g) Claim 16 of the '920 patent recites: "The semiconductor structure of claim 14, wherein a first semiconductor device is situated in said first region of said at least one crystalline epitaxial layer and a second semiconductor device is situated in said second region of said at least one crystalline epitaxial layer." *Id.*

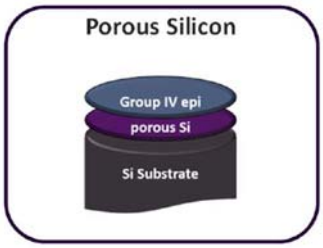
(h) Claim 19 of the '920 patent recites: "The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor that is utilized in a radio frequency (RF) switch." *Id.*

47. The form and function of the semiconductor structures contemplated by the '920 patent and recited in its claims were devised as part of the collaboration with IQE, and which are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, CMOS compatible epitaxy on porous silicon, and applications for localized RF devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims in the '920 patent. Indeed, in a correspondence between Richard Hammond of IQE and Edward

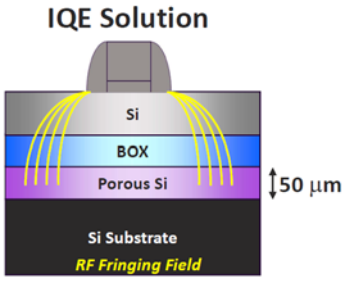
Preisler of Tower on November 7, 2018, Richard Hammond proposed a "[l]ocalized porous demonstrator…to expose localized areas for subsequent thick porous silicon



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

formation…[i]nductors on selective porous regions." (Confidential Exhibit 9, Pg. 1.)

48. Furthermore, a stated goal of the '920 patent is to create semiconductor dies with "reduced RF signal leakage, reduced need for numerous body contacts, and increased heat dissipation at low cost." Exhibit 3. These include advantages presented by IQE to Tower during at least one of the confidential meetings between the parties. For example, their 2019 Presentation describes suppressing a "RF fringing field" due to properties of the porous layer that had "[s]ignificantly improved harmonics" and "[i]mproved cross talk compared to Trap-rich HR-Si." (Confidential Exhibit 7, Pgs. 14-15.) Improved signal leakage was one of the expected benefits from the collaboration.

49. IQE's inventors of the porous silicon technology continued to share positive test results with Tower. The mutual NDA was still in place during these conversations, as Tower and IQE were considering collaborations for other projects.

50. On December 4, 2019, Tower applied for a third patent related to IQE's porous silicon technology—the '572 patent—naming David J. Howard as the sole inventor. The '572 patent is attached as Exhibit 4 to this Complaint and is incorporated by reference. The very next day, David Howard emailed IQE employees, including Wayne Johnson, asking for further meetings and information

and noting that David Howard had been "observing progress on porous Si discussions" on an ongoing basis.

51. The '572 patent sought to leverage porous silicon to "withstand thermal and mechanical stresses" and further misappropriated IQE's trade secrets in its claims. Exhibit 4. All claims of the '572 patent recite porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '572 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations between the parties.

52. Specifically, at least claims 1, 2, 13, and 14 of the '572 patent claim proprietary trade secrets that IQE communicated to Tower and the named inventor:

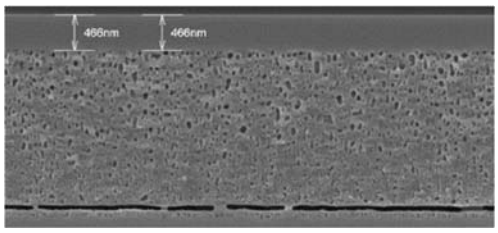
(a) For example, claim 1 of the '572 patent recites: "A semiconductor structure comprising: a semiconductor substrate; a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material; a through-substrate via (TSV) within said porous semiconductor region; said porous semiconductor region causing said semiconductor structure and/or said TSV to withstand thermal and mechanical stresses." Exhibit 4.

(b) Claim 2 of the '572 patent recites: "The semiconductor structure of claim 1, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is significantly greater than a second CTE of said semiconductor substrate." *Id.*

(c) Claim 13 of the '572 patent recites: "A semiconductor structure comprising: a semiconductor substrate; a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material; a through-substrate via (TSV) at least partially within said porous semiconductor region; said porous semiconductor region causing said semiconductor structure to withstand thermal or mechanical stress." *Id.*

(d) Claim 14 of the '572 patent recites: "The semiconductor structure of claim 13, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is greater than a second CTE of said semiconductor substrate." *Id.*

53. The form and function of the semiconductor structures contemplated



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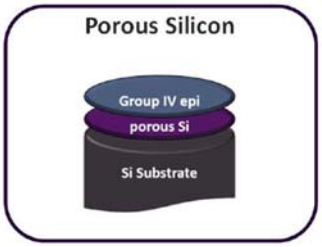
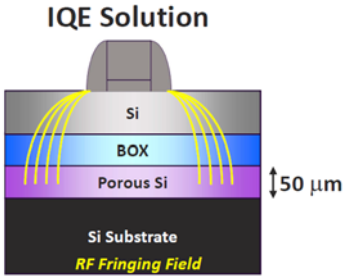


Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

by the '572 patent and recited in its claims are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, CMOS compatible epitaxy on porous silicon, and applications for RF devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims in the '572 patent. Indeed, the 2018 Presentation stated "CMOS Fab compatible" and the 2019 Presentation stated "CMOS Processing Compatible." *See* Confidential Exhibit 6, 7. Further, in a correspondence between Richard Hammond of IQE and Edward Preisler and Paul D. Hurwitz of Tower on November 13, 2018 ("2018 Response"), Richard Hammond discussed an "STI [shallow trench isolation] module…STI etch will consume the 1450A body and penetrate into the porous region." (Confidential Exhibit 9, Pg. 1.)

54. In addition, the MOU between the parties stated "[m]echanical strength is expected to be compromised Vs c-Si substrates, and the *large TCE mismatch* between c-Si [crystalline silicon] and p-Si [porous silicon] may limit thermal ramp

rates…may need to improve mechanical parameters such as bow and warp." *See* Confidential Exhibit 11.

55. On August 12, 2021, Tower once again applied for a patent based on IQE's trade secrets disclosed during the negotiations with IQE—the '712 application. This application seeks to patent methods of forming semiconductor structures using porous silicon in RF devices using the concepts initially disclosed to Tower by IQE. A copy of the '712 application is attached to this Complaint as Exhibit 5 and is incorporated by reference.

56. All claims of the '712 application thus recite porous semiconductor technology and methods developed by IQE. The entirety of the invention claimed in the '712 application was derived from IQE's trade secrets conveyed to Tower during negotiations between the parties.

57. Specifically, at least claims 14-19, 22-25, 27, 28, and 30-32 of the '712 application claim proprietary trade secrets that IQE communicated to Tower and the named inventor:

(a) For example, claim 14 of the '712 application recites: "A method comprising: forming a crystalline epitaxial layer over a porous semiconductor layer, said porous semiconductor layer being situated over a substrate; forming a first semiconductor device in said crystalline epitaxial layer; said substrate having a first dielectric constant, and said porous semiconductor layer having a. second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 5.

(b) Claim 15 of the '712 application recites: "The method of claim 14, further comprising annealing said porous semiconductor layer prior to said forming said crystalline epitaxial layer." *Id.*

(c) Claim 19 of the '712 application recites: "The method of claim 14, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(d) Claim 22 of the '712 application recites: "A method comprising: forming at least one crystalline epitaxial layer over a porous silicon layer in a semiconductor structure; forming first and second transistors and an electrical isolation region separating said first and second transistors in said at least one crystalline epitaxial layer." *Id.*

(e) Claim 23 of the '712 application recites: "The method of claim 22, further comprising forming said porous silicon layer over a bulk silicon substrate prior to said forming said at least one crystalline epitaxial layer." *Id.*

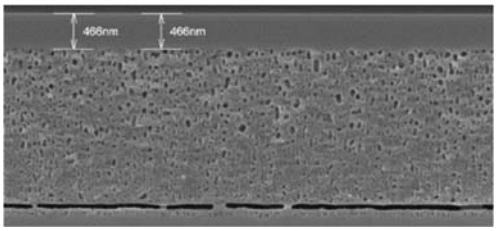
(f) Claim 27 of the '712 application recites: "A method comprising: forming a porous semiconductor layer over a substrate, said porous semiconductor layer having a higher resistivity that said substrate; forming at least one crystalline epitaxial layer over said porous semiconductor layer; forming a first semiconductor device in said at least one crystalline epitaxial layer." *Id.*

(g) Claim 28 of the '712 application recites: "The method of claim 27, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material." *Id.*

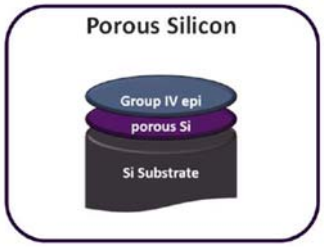
(h) Claim 32 of the '712 application recites: "The method of claim 27, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

58. Similar to the '740 patent, the form and function of the semiconductor structures and methods contemplated by the '712 application and recited in its claims are identical to the porous semiconductor structures and methods which are IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, epitaxy on porous silicon, and applications for RF

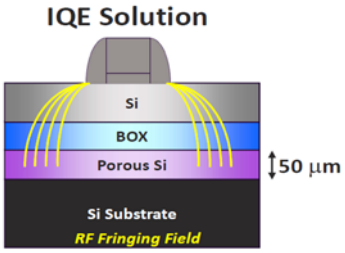
devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

in the '712 application. Indeed, the 2019 Presentation stated "[p]orous Si for RF Switches…[s]ignificantly improved harmonics…[n]o change in device architecture." (Confidential Exhibit 7, Pg. 14.)

59. In addition, the 2019 Presentation stated IQE's porous silicon technology was "CMOS Processing Compatible" and that there was "[n]o degradation with *annealing*." (Confidential Exhibit 7, Pg. 16 (emphasis added).) Moreover, in the 2018 Response, Richard Hammond of IQE stated "[t]he wafers that we provide will have undergone a *pre-epi flash off* [anneal] in excess of 1100C." (Confidential Exhibit 9, Pg. 1 (emphasis added).)

60. IQE was unaware of Tower's conduct until the patent applications were published. Tower never informed IQE that it filed these patent applications. Three of the patent applications were published on the same day April 15, 2021, and the remaining application, the '712 application, was published on December 2, 2021. IQE only found out about Tower's actions upon seeing these published applications.

61. Tower sought to secure an advantageous market system by entering into an exclusive contract with IQE, in order to benefit from IQE's trade secrets. Indeed, Tower insisted on exclusivity as essential to any supplier agreement with IQE. IQE's refusal to agree to that exclusivity contributed to the breakdown of the negotiations. *See* Confidential Exhibit 10.

62. Had Tower been the true inventor of the technology now claimed in its patents and application, it would not have needed exclusivity through contract. There is no reason to insist on contractual exclusivity where exclusive rights are secured through patents. Tower's behavior confirms that it did not believe itself to have exclusive rights to IQE's porous silicon technology.

63. Having been denied an exclusive deal with IQE, Tower now seeks to gain by deception what it could not gain through negotiation and contractual agreement. By using patent rights to gain exclusive rights to IQE's trade secrets, Tower looks to force IQE's hand, compelling it to deal with Tower—and Tower alone—in order to practice its own technology.

64. Since learning of Tower's patents directed to IQE's porous silicon technology, and thus Tower's misconduct, IQE has diligently pursued its legal interests, including by filing this Complaint.

COUNT I

Violation of the Defend Trade Secrets Act (18 U.S.C. § 1836 et seq.)

65. IQE incorporates by reference each and every allegation contained in paragraphs 1–64 above as if fully set forth herein.

66. Between October 2018 and February 2020, IQE and Tower were engaged in negotiations surrounding a potential collaboration between the two companies in which Tower repeatedly sought exclusive access to IQE's trade secrets including, but not limited to, the following: manufacture and use of porous silicon wafers, III-V materials on silicon-germanium alloys, rare earth material filters, and advanced III-V power devices.

67. During these negotiations, IQE provided Tower with information pertaining to a number of IQE trade secrets in the form of presentations, experimental data, and detailed descriptions of the composition of IQE's wafers.

68. On October 9, 2019, October 10, 2019, and December 4, 2019, while negotiations with IQE were still ongoing, Tower applied for the '740, '920, and '572 patents.

69. On August 12, 2021, Tower filed for another patent: the '712 application.

70. These patents and patent application all claim a "semiconductor structure comprising: . . . porous silicon," and recite in their specifications and claims proprietary trade secrets that Tower had obtained from the negotiations with IQE and under a duty of confidentiality.

71. This disclosure and use of IQE's trade secrets amounts to misappropriation under 18 U.S.C. § 1836(b)(1).

72. IQE took great care to safeguard its trade secrets, only disclosing them to IQE personnel and as needed for its legitimate business interests. Materials containing trade secrets were marked as confidential and kept secret. When disclosed to Tower, IQE took care to ensure they were only disclosed under a strict NDA. Moreover, IQE repeatedly reminded Tower of the receiver's obligation of confidentiality.

73. Tower has copied IQE's valuable trade secrets, incorporated them into Tower's patents and patent application, is using them, and intends to continue using them to further its business interests and to damage IQE's market standing.

74. IQE did not authorize or consent to Tower or anyone else using its trade secrets. IQE's disclosure of the protected information was strictly confidential and subject to an NDA. Tower was aware that it had received IQE's trade secrets and made clear that it understood that it was under an obligation not to disclose those secrets or appropriate the information therein for its own benefit.

75. Prior to the acts complained of herein, IQE's trade secrets had, and continue to have, independent economic value deriving from the fact that such information is not readily ascertainable through proper means nor known to IQE's

competitors, their customers, or the public at large who could obtain economic value from their use or disclosure.

76. Tower has used IQE's trade secrets to obtain patents on IQE's technology, including the '740, '920, and '572 patents, and the '712 application. This misappropriation has destroyed the secrecy of this information. Any enforcement of Tower's ill-gotten patents will prevent IQE from freely practicing its own technology. The existence of the patents themselves has an immediate and ongoing pronounced chilling effect on IQE's ability to market its technology to other customers.

77. The applications that issued as the '740, '920, and the '572 patents were published on April 15, 2021. The '712 application was published on December 2, 2021.

78. IQE discovered these patent applications, and thus discovered Tower's misappropriation of IQE's trade secrets, on February 14, 2022, as part of its routine diligence. IQE has brought this action within the three-year period prescribed by 18 U.S.C. § 1836(d), and its claims are not time barred.

79. As a direct and proximate result of Tower's misappropriation and use of IQE's trade secrets, IQE has suffered irreparable harm subject to proof at trial.

80. In addition to said damages, Tower has been unjustly enriched by its misappropriation and use of IQE's trade secrets.

81. Tower's misappropriation of IQE's trade secrets was willful and malicious, so as to justify an award of additional punitive damages pursuant to 18 U.S.C. § 1836(b)(3)(C), in a sum sufficient to punish Tower and deter others from engaging in similar misconduct.

82. Because the misappropriation by Tower was willful and malicious, IQE is also entitled to an award of reasonable attorney's fees and costs incurred during litigation pursuant to 18 U.S.C. § 1836 (b)(3)(D).

83. IQE is further entitled to an order enjoining Tower from further using IQE's trade secrets to unfairly compete with IQE, and to an order further compelling Tower to turn over to IQE all copies of IQE's trade secrets in their possession, custody, or control.

COUNT II:

Violation of California Trade Secrets Act (Cal. Civ. Code § 3246 et seq.)

84. IQE incorporates by reference each and every allegation contained in paragraphs 1–83 above as if fully set forth herein.

85. Between October 2018 and February 2020, IQE and Tower were engaged in negotiations surrounding a potential collaboration between the two companies in which Tower repeatedly sought exclusive access to IQE's trade secrets including, but not limited to, the following: manufacture and use of porous silicon wafers, III-V materials on silicon-germanium alloys, rare earth metal filters, and advanced III-V power devices.

86. During these negotiations, IQE provided Tower with information pertaining to a number of IQE trade secrets in the form of presentations, experimental data, and detailed technical description of the composition of IQE's wafers.

87. On October 9, 2019, October 10, 2019, and December 4, 2019, while negotiations with IQE were still ongoing, Tower applied for '740, '920, and '572 patents.

88. On August 12, 2021, Tower filed for another patent: the '712 application.

89. These patents and patent application all claimed a "semiconductor structure comprising: . . . porous silicon," and recite in their specifications and claims proprietary trade secrets that Tower obtained from the negotiations with IQE and under a duty of confidentiality.

90. This disclosure and use of IQE's trade secrets amounts to misappropriation under Cal. Civ. Code § 3426.1(b).

91. IQE took great care to safeguard its trade secrets, only disclosing them to IQE personnel and as needed for its legitimate business interests. Materials containing trade secrets were marked as confidential and kept secret. When disclosed to Tower, IQE took care to ensure they were only disclosed under a strict NDA. Moreover, IQE repeatedly reminded Tower of the receiver's obligation of confidentiality.

92. Tower has copied IQE's trade secrets, incorporated them into Tower's patents and patent application, is using them, and intends to continue using them to further their business interests and to damage IQE's market standing.

93. IQE did not authorize or consent to Tower or anyone else using its trade secrets. IQE's disclosure of the protected information was strictly confidential and subject to an NDA. Tower understood that it had received IQE's trade secrets and understood that it was under an obligation not to disclose those secrets or appropriate the information therein for its own benefit.

94. Prior to the acts complained of herein, IQE's trade secrets had, and continue to have, independent economic value deriving from the fact that such information is not readily ascertainable through proper means nor known to IQE's competitors, their customers, or the public at large who could obtain economic value from their use or disclosure.

95. Tower has used IQE's trade secrets in the patenting of the subject matter claimed in the '740, '920, and '572 patents, and the '712 application. The result of this misappropriation is to prevent IQE from practicing its own technology independently of Tower.

96. IQE discovered Tower's misappropriation of IQE's trade secrets in 2022, shortly after Defendant's patent applications were published in April and

December of 2021. IQE has brought this action within the three-year period prescribed by Cal. Civ. Code § 3426.6, and its claims are not time barred.

97. As a direct and proximate result of Tower's misappropriation and use of IQE's trade secrets, IQE has suffered irreparable damages in an amount exceeding the minimum jurisdictional limits of this Court and subject to proof at trial.

98. In addition to said damages, Tower has been unjustly enriched by the misappropriation and use of IQE's trade secrets.

99. Tower's misappropriation of IQE's trade secrets was willful and malicious, so as to justify an award of additional exemplary damages pursuant to Cal. Civ. Code § 3426.3(c), in a sum sufficient to punish Tower and deter other from engaging in similar misconduct.

100. Because the misappropriation by Tower was willful and malicious, IQE is also entitled to an award of reasonable attorney's fees and costs incurred during litigation pursuant to Cal. Civ. Code § 3426.4.

101. IQE is further entitled to an order enjoining Tower from further using IQE's trade secrets to unfairly compete with IQE, and to an order further compelling Tower to turn over to IQE all copies of IQE's trade secrets in their possession, custody, or control.

COUNT III:

Correction of Inventorship (35 U.S.C. § 256)

102. IQE incorporates by reference each and every allegation contained in paragraphs 1–101 above as if fully set forth herein.

103. Since beginning negotiations with IQE, Tower has applied for 4 patents relating to porous silicon semiconductors: the '740, '920, and '572 patents and the '712 application.

104. Claims 1 and 8 of the '740 patent are representative.

(a) Claim 1 recites: "A semiconductor structure comprising: a substrate having a first dielectric constant; a porous semiconductor layer situated over said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer; said porous semiconductor layer having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 2.

(b) Claim 8 recites: "A semiconductor structure comprising: a porous silicon layer; at least one crystalline epitaxial layer situated directly on said porous silicon layer; first and second transistors situated in said at least one crystalline epitaxial layer; an electrical isolation region separating said first and second transistors." *Id.*

105. These claims encompass the proprietary porous silicon and crystalline epitaxial layer technologies that were disclosed to Tower through the specific named inventors on the patents and patent application in question, who are its agents. These named inventors are Paul D. Hurwitz, Edward Preisler, David Howard, and Marco Racanelli.

106. Throughout their negotiations, Tower repeatedly and explicitly showed particular interest in obtaining exclusive access to RF applications of IQE's porous silicon and crystalline epitaxial wafers, products that Tower did not manufacture. Specifically, Tower wanted exclusivity for porous RF switches (the subject matter later claimed in the '740 patent and '712 application) and localized patterning of porous regions (the subject matter later claimed in the '920 patent).

107. During the period in which Tower was applying for the patents and immediately preceding this timeframe, in response to Tower's requests and in good faith, IQE provided the named inventors with technical information, experimental

data, explanations of various features of the technology, as well as answered questions from the named inventors.

108. Richard Hammond, Rodney Pelzel, and Andrew Clark have each been employees of IQE since 2016 or earlier and had previously assigned all right and title to their inventions and work to IQE.

109. Tower's sudden patenting of the same technology they were attempting to negotiate an exclusive access deal for was not independent of Richard Hammond, Rodney Pelzel, and Andrew Clark's work, as the patents were derived from the information provided to them by Richard Hammond, Rodney Pelzel, and Andrew Clark through the open line of communication by which the parties discussed their ongoing business relationship.

110. On information and belief, Tower did not and does not have any independent research capabilities regarding porous Si technology and was not aware of the technical features of IQE's porous Si products and processes until that information was communicated to Tower through its NDA-protected meetings with IQE.

111. IQE's contributions to the '740, '920, and '572 patents, and '712 application amounted to the entire conception and reduction to practice of the inventions in question, including an epitaxial layer on porous silicon and incorporating a semiconductor device in the epitaxial layer. IQE provided the named inventors with far more than well-known principles, nor did Richard Hammond, Rodney Pelzel, and Andrew Clark merely explain the state of the art. When measured against the full inventions, Richard Hammond, Rodney Pelzel, and Andrew Clark's work contributed substantially to both the conception and reduction to practice of the inventions claimed in all three patents and the patent application.

112. Neither Richard Hammond, Rodney Pelzel, or Andrew Clark, nor any other member of IQE is listed on any of the patents or patent applications as an inventor. Furthermore, the patents are solely assigned to Newport Fab, LLC.

113. The first of these patents was applied for on October 9, 2019, and was published on April 15, 2021. Before April 2021, there was no reasonable diligence which could have uncovered Tower's wrongdoing, thus April 2021 should be considered the date of discovery.

114. Thus this action has been brought before six years have passed since IQE knew or reasonably should have known of Tower's wrongdoing, and Tower is not entitled to a presumption of laches.

115. IQE's and IQE's employees' absence from the patents in question was not due to any deceptive intent on the part of IQE or its employees.

116. Due to the substantial contributions by Richard Hammond, Rodney Pelzel, and Andrew Clark upon which Paul Hurwitz, Edward Preisler, David Howard, and Marco Racanelli depended, IQE is entitled to a correction of inventorship to include (1) add Richard Hammond, Rodney Pelzel, and Andrew Clark and (2) remove the currently named inventors.

117. Further, IQE is entitled to injunctive relief in the form of an order for Tower to cease and desist from practicing the patents in question, and from further use of the misappropriated trade secrets when pursuing patents in the future.

COUNT IV:

Breach of Contract

118. IQE incorporates by reference each and every allegation contained in paragraphs 1–117 above as if fully set forth herein.

119. Among other agreements, IQE signed a mutually binding Non-Disclosure Agreement effective November 12, 2015, with Tower, which also bound its affiliates such as Newport Fab, LLC (then Jazz Semiconductor Inc). *See* Exhibit 1.

120. This NDA imposed a duty on both parties to protect any "Confidential Information" which is defined in the NDA to include "all information, documents, data, reports, interpretations, forecast, analyses, compilations, studies, ideas,

inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the Disclosing Party to the receiving party," for a period of at least five years from the date of disclosure. *Id.*

121. During their negotiations, and beginning on November 6, 2018, IQE disclosed Confidential Information relating to their trade secrets and to their porous silicon wafers in particular.

122. By using and disclosing this information to pursue a patent on porous silicon semiconductors, Tower breached its contractual duty with IQE.

123. Therefore, IQE is entitled to damages and injunctive relief due to Tower's breach of the NDA.

COUNT V:

Violation of California Unfair Competition Law (Cal. Bus. And Professions Code § 17200)

124. IQE incorporates by reference each and every allegation contained in paragraphs 1–123 above as if fully set forth herein.

125. On a date that is currently unknown, but while the negotiations with IQE were still ongoing, Tower began a course of conduct consisting of actions of unfair competition as defined by California Business and Professions Code § 17200, by engaging in the practices herein described, including filing multiple patent applications with the USPTO disclosing and claiming IQE's trade secret and proprietary technology.

126. Tower's acts violate the California Business and Professions Code § 17200 in that Tower misappropriated and misused IQE's proprietary information and intellectual property, fraudulently negotiated with IQE to gain access to their trade secrets, and used IQE's proprietary information for their own benefit and without the consent of IQE.

127. The harm to IQE, IQE's customers, and the public at large outweighs any potential utility of Tower's conduct.

128. Tower's actions herein described constitute unlawful, unfair, and fraudulent business practices within the meaning of California Business Code § 17200, which pose a threat, and will continue to pose a threat to IQE and to IQE's customers.

129. As a direct result of the aforementioned acts, IQE is entitled to injunctive relief as may be necessary to prevent the use or employment of said unfair business practices, and an order of restitution compelling Tower to disgorge the profits which resulted from their wrongdoing.

COUNT VI:

Intentional Interference with Prospective Economic Advantage

130. IQE incorporates by reference each and every allegation contained in paragraphs 1–129 above as if fully set forth herein.

131. IQE has developed numerous business and contractual relationships with existing and potential customers, based on their ability to provide unique and custom semiconductor solutions by using their proprietary systems and technology. These relationships carried with them the probability of future economic benefit to IQE.

132. Tower has, and at all relevant times herein alleged had, knowledge of the existence of IQE's business and contractual relations. Indeed, a sticking point of negotiations between IQE and Tower is that IQE planned and worked to continue to solicit these potential customers and thus rejected Tower's request for an exclusive arrangement.

133. In the past, Tower sought to secure an advantageous market system by entering into an exclusive contract with IQE, in order to benefit from IQE's trade secrets. Indeed, Tower insisted on exclusivity as essential to any supplier agreement.

134. Had Tower been the true inventor of the technology now claimed in its patents, it would not have needed exclusivity through contract. There is no reason to insist on contractual exclusivity where exclusive rights are secured through patents. Tower's behavior confirms that it did not believe itself to have exclusive rights to IQE's porous silicon technology.

135. Having been denied an exclusive deal with IQE, Tower now seeks to gain by deception what it could not gain through negotiation. By using patent rights to gain exclusive rights to IQE's trade secrets, Tower looks to force IQE's hand, compelling it to deal with Tower—and Tower alone—in order to practice its own technology.

136. Furthermore, a core of IQE's business is the development of unique and custom semiconductor solutions for customers. For that reason, customers not only engage IQE based on their current portfolio of solutions but also on the basis of prospective technologies that IQE can develop. The existence of these patents disrupts IQE's ability to innovate compound semiconductors integrating porous silicon, and other prospective solutions that use porous silicon and crystalline epitaxy, substantially disrupting IQE's market position and trajectory.

137. Beyond the patents and patent application in question, the unlawful disclosures of IQE's trade secrets alone disrupts IQE's business relations with current and prospective customers by enabling others to compete with IQE using the trade secret information disclosed in the patents to replicate IQE's products. Additionally, the threat of enforcement of Tower's patents against IQE or its customers undermines IQE's ability to freely offer its technology in the marketplace.

138. As a proximate result of Tower's interference with IQE's prospective economic advantage, IQE's customer relationships have been disrupted. IQE's ability to compete in the marketplace for porous silicon has been damaged. IQE is

entitled to recover compensatory damages in an amount exceeding the minimum jurisdictional limit of this Court and subject to proof at trial.

139. Tower's acts were willful and malicious insofar as Defendants committed such acts with the intent to injure IQE's business, and to increase their own profits with conscious disregard for IQE's rights, thereby warranting an award of punitive damages in an amount sufficient to punish Tower and deter others from engaging in similar misconduct.

COUNT VII:

Negligent Interference with Prospective Economic Advantage

140. IQE incorporates by reference each and every allegation contained in paragraphs 1–139 above as if fully set forth herein.

141. In engaging in the conduct and actions described herein, Tower also negligently interfered with IQE's existing business relationships with customers and undermined or interfered with the acquisition of new customers, all of which carried the probability of future economic benefit to IQE.

142. As a proximate result of the wrongful acts herein alleged, IQE has been damaged in an amount exceeding the minimum jurisdictional limit of this Court and subject to proof at trial.

PRAYER FOR RELIEF

WHEREFORE, IQE prays for judgment against Tower as follows:

1. For injunctive relief in the form of a correction of inventorship of the U.S. Patent Nos. 11,164,740, 11,195,920, and 11,145,572 and U.S. Patent Application 17/400,712;

2. For compensatory damages in a sum according to proof;

3. For the statutory remedies specified in the Defend Trade Secrets Act and the California Uniform Trade Secrets Act, including the recovery of an amount equal to Tower's unjust enrichment and any reasonable royalties the Court deems necessary and appropriate;

4. For punitive damages in a sum according to proof;

5. For the contractual damages for breach of the parties' NDA;

6. For an award of attorney's fees as permitted under the Defend Trade Secrets Act and the California Uniform Trade Secrets Act;

7. For interest at the legal rate;

8. For an order enjoining Tower and their agents, servants, employees, employers, and all persons acting under, in concert with, of or for them from further using or soliciting customers based on their wrongful possession of IQE's trade secrets;

9. For an order declaring that Tower and their agents, servants, employees, employers, and all persons acting under, in concert with, of or for them, are preliminarily and permanently enjoined from acts constituting a violation of the Defend Trade Secrets Act, the California Uniform Trade Secrets Act, and the California Unfair Competition Statute, including the misappropriation of trade secrets, pursuant to 18 U.S.C § 1836(b)(3)(A), CA Civ. Code § 3246.5, and the equitable powers of the Court;

10. For the costs incurred in this action; and

11. For such other and further relief as the Court deems just and proper.

DATED: APRIL 25, 2022

KARIN G. PAGNANELLI
MITCHELL SILBERBERG & KNUPP LLP

By: /s/ Karin G. Pagnanelli
Karin G. Pagnanelli (SBN 174763)
Attorneys for Plaintiff
IQE, plc

JURY DEMAND

IQE demands a trial by jury on all matters alleged herein in accordance with the Seventh Amendment to the U.S. Constitution and Rule 38(b) of the Federal Rules for Civil Procedure.

DATED: APRIL 25, 2022

KARIN G. PAGNANELLI
MITCHELL SILBERBERG & KNUPP LLP

By: /s/ Karin G. Pagnanelli
Karin G. Pagnanelli (SBN 174763)
Attorneys for Plaintiff
IQE, plc

Exhibit 1

TOWERJAZZ

Non-Disclosure Agreement

Effective Date: 11th November 12, 2015.

In order to protect certain confidential information, **Tower Semiconductor Ltd.** whose principal address is Ramat Gavriel Industrial Park, P.O. Box 619 Migdal Haemek 23105, Israel and its affiliates, including **Jazz Semiconductor, Inc.** whose principal address is 4321 Jamboree Road, Newport Beach, CA 92660, USA and **TowerJazz Panasonic Semiconductor Co., Ltd.** whose principal address is 800 Higashiyama, Uozu City, Toyama 937-8585, Japan (collectively, "TowerJazz") as one party, and IQE plc, , whose principal address is Pascal Close, St Mellons, Cardiff, Wales, UK CF3 0LW (the "Customer") as the other party, hereby enter into this Non-Disclosure Agreement ("Agreement") and agree that:

1. "Confidential Information" (also referred to as "CI") means all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates (the "Disclosing Party"), provided by the Disclosing Party to the receiving party (the "Recipient"), as well as all information in tangible form that bears a "confidential," "proprietary," "secret," or similar legend, and discussions relating to that information whether those discussions occur prior to, concurrent with, or following disclosure of the information. The Disclosing Party shall make reasonable efforts to mark its Confidential Information in tangible form with any of the aforementioned legends prior to disclosure. However, the Disclosing Party's information in tangible form that does not bear any of these legends, and discussions relating to that information, shall nevertheless be protected hereunder as Confidential Information, if the Recipient knew, or should have reasonably known under the circumstances, that the information is confidential or if such information had been communicated in confidence. Confidential Information shall also include, without limitation, all information obtained by Recipient from any website hosted by or on behalf of the Disclosing Party that is not accessible to the general public but is accessible via a password and user name.

2. The Recipient shall not disclose CI to any third party (except as provided herein below) and shall make use of CI only for wafer manufacturing at TowerJazz, including related processes and services (the "Purpose").

3. The Recipient's duties hereunder expire 5 years from the date of disclosure. However, subject to section 5 below, the confidentiality obligation to protect TowerJazz's design kits (including design rules, EDA and PDK documentations and run sets) shall not expire.

4. Recipient shall protect the disclosed CI from any unauthorized use, dissemination or publication using the same degree of care Recipient uses to protect its own information of a like nature and sensitivity, but no less than a reasonable degree of care. Recipient will not disclose any of the Disclosing Party's CI, except to its employees, bankers, accountants, attorneys, consultants or subcontractors who have a need to know for the Purpose and who agree to abide by nondisclosure terms at least as comprehensive as those set forth herein.

5. This Agreement imposes no obligation upon Recipient to the extent any CI (a) was rightfully in Recipient's possession before receipt thereof under this Agreement; (b) is generally available to the public at the time of disclosure or becomes public knowledge through no fault of Recipient; (c) is rightfully received by Recipient from a third party without a duty of confidentiality; or (d) was independently developed by Recipient without use of the Confidential Information received from the Disclosing Party, as evidenced in writing. Recipient may disclose CI to the extent required by any law, regulation or other applicable judicial or governmental order. Unless legally prohibited, Recipient will timely notify the Disclosing Party of such disclosure requirement in advance of the required disclosure so as to allow the Disclosing Party the opportunity to oppose or limit such disclosure.

6. Each Disclosing Party warrants that it has the right to make the disclosures made under this Agreement. NO OTHER WARRANTIES ARE MADE BY EITHER PARTY UNDER THIS AGREEMENT. ANY INFORMATION EXCHANGED UNDER THIS AGREEMENT IS PROVIDED "AS IS".

7. Neither party acquires any intellectual property rights under this Agreement. The CI of Disclosing Party shall remain the property of the Disclosing Party, and shall be returned to the Disclosing Party promptly upon written request, or destroyed at the Disclosing Party's option. Recipient agrees to promptly provide written confirmation to Disclosing Party of its compliance with any such request.

8. This Agreement imposes no obligations on either party to purchase, sell, license, transfer or otherwise dispose of any technology, service or products or enter into any other business relationship with the other party.

9. The Recipient acknowledges its obligations to control access to technical data under the U.S. Export Administration laws and regulations and/or other applicable local regulations and agrees to adhere to such laws and regulations with regard to any CI received under this Agreement. Recipient will not export outside the United States, if a United States company or citizen, or re-export, if a foreign company or citizen, except as permitted by said laws and regulations.

CUSTOMER HEREBY DECLARES THAT THE CONFIDENTIAL INFORMATION (CHECK ONE):

X Is not intended to design product(s) for use with, derived from, or developed specifically for a military application or any radiation hardened or space application, or for use in any such item.

☐ Is intended to design product(s) for use with, derived from, or developed specifically for military application or any radiation hardened or space application, or for use in any such item.

10. It is understood and agreed that the unauthorized use or disclosure of any CI may cause irreparable harm to the Disclosing Party. Accordingly, Recipient agrees that the Disclosing Party will have the right to seek an immediate injunction against any breach or threatened breach of this Agreement without the need for proof of actual damages, as well as the right to pursue any and all other rights and remedies available at law or in equity for such a breach.

11. No failure or delay in exercising any right, power or privilege hereunder shall operate as a waiver thereof, nor shall any single or partial exercise thereof preclude any future exercise thereof or any exercise thereof under applicable law or in equity. This Agreement is the entire and only agreement between the parties hereto with respect to its subject matter, and supersedes all prior and contemporaneous understandings, discussions and agreements with respect to such subject matter. All additions or modifications to this Agreement must be made in writing and agreed to by both parties. This Agreement may be executed in counterparts. This Agreement may not be assigned by either party without the other party's prior written consent.

12. This Agreement, as well as any disputes arising out of or relating to this Agreement, shall be interpreted under and governed by the laws of the State of California. Any disputes arising out of or relating to this Agreement and not resolved by the parties themselves shall be commenced solely in the federal or state courts located within the State of California. In such event, each party irrevocably agrees to submit to the personal jurisdiction of such courts and irrevocably waives any objection to such venue. The parties agree that the State of California has a reasonable relationship to the subject matter of this Agreement and that there is a reasonable basis for the selections of governing law and venue set forth above.

TowerJazz

Signature: [signature]

By: Zmira Luvic
Title: GM TOPS BU

Company: IQE plc.

Signature: [signature]

By: Drew Nelson
Title: President /CEO.

Exhibit 2

US011164740B2

(12) **United States Patent**
Hurwitz et al.

(10) **Patent No.: US 11,164,740 B2**
(45) **Date of Patent: Nov. 2, 2021**

(54) **SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR LAYER FOR RF DEVICES**

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(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/597,779**

(22) Filed: **Oct. 9, 2019**

(65) **Prior Publication Data**

US 2021/0111019 A1 Apr. 15, 2021

(51) **Int. Cl.**

H01L 21/02	(2006.01)
H01L 29/04	(2006.01)
H01L 29/08	(2006.01)
H01L 23/66	(2006.01)
H03K 17/687	(2006.01)
H01L 21/762	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 21/02203*** (2013.01); ***H01L 21/76294*** (2013.01); ***H01L 23/66*** (2013.01); ***H01L 29/04*** (2013.01); ***H01L 29/0843*** (2013.01); ***H03K 17/687*** (2013.01); *H01L 2223/6677* (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/02203; H01L 21/76294; H01L 29/04; H01L 29/0843; H01L 23/66; H01L 17/687; H01L 27/687; H01L 2223/6677; H01L 21/02; H01L 29/08; H01L 21/762; H03K 17/687

USPC 257/728

See application file for complete search history.

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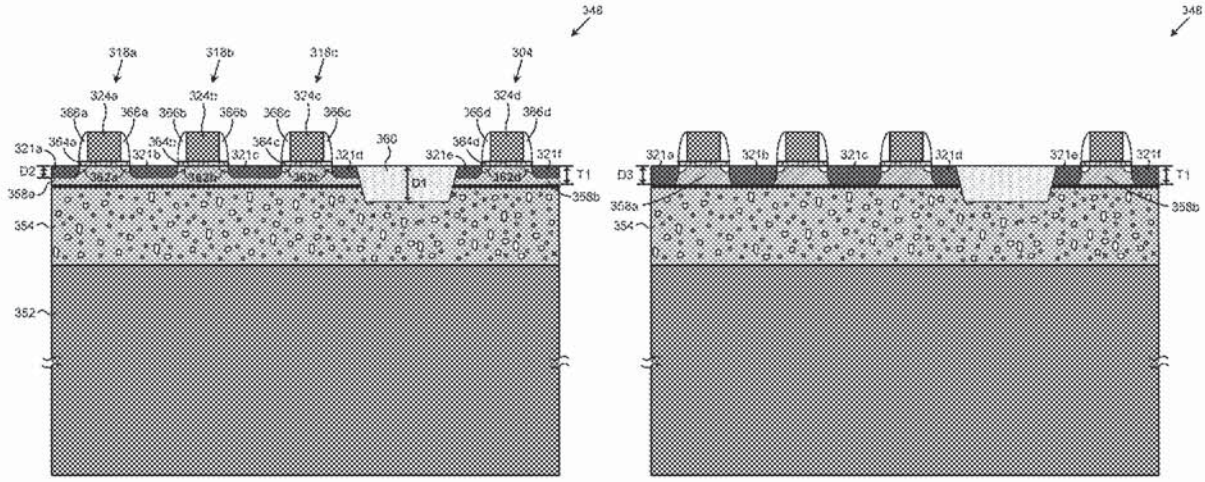
Primary Examiner — Alexander O Williams
(74) *Attorney, Agent, or Firm* — Farjami & Farjami LLP

(57) **ABSTRACT**

A semiconductor structure includes a substrate having a first dielectric constant, a porous semiconductor layer situated over the substrate, and a crystalline epitaxial layer situated over the porous semiconductor layer. A first semiconductor device is situated in the crystalline epitaxial layer. The porous semiconductor layer has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor layer reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer, and an electrical isolation region separating the first and second semiconductor devices.

20 Claims, 8 Drawing Sheets



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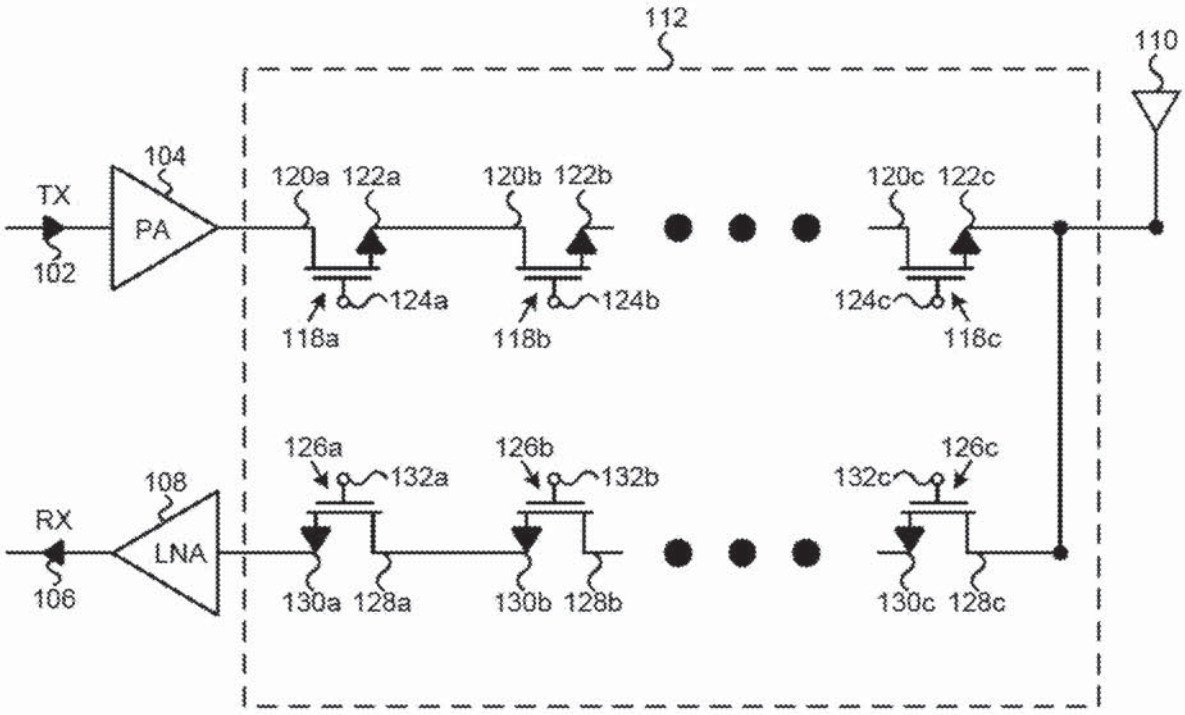

112
110
104
TX
PA
102
120a 122a
120b 122b
120c 122c
124a
124b
124c
118a
118b
118c
126a
126b
126c
132a
132b
132c
108
RX
LNA
106
130a 128a
130b 128b
130c 128c

FIG. 1

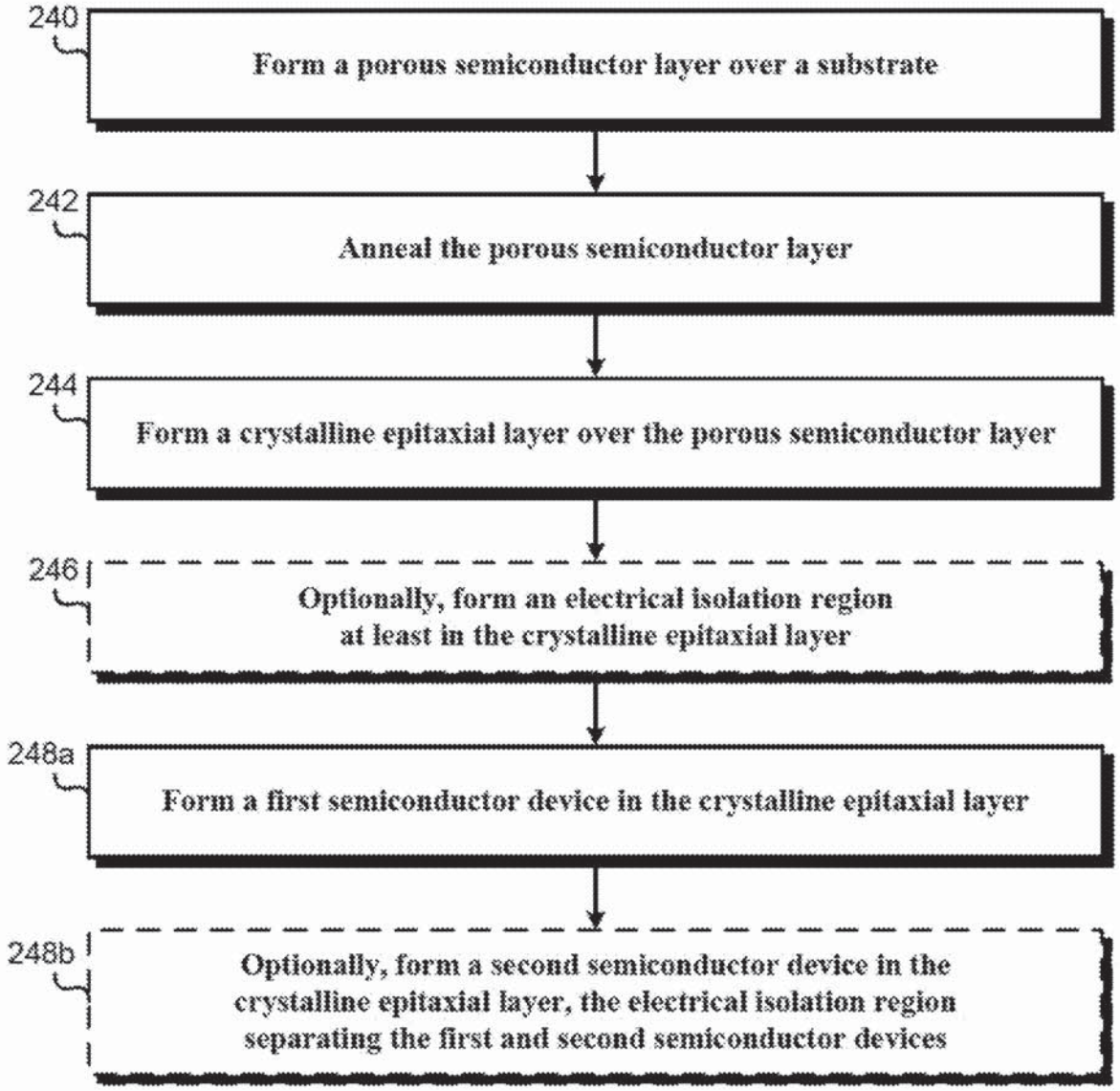

240
Form a porous semiconductor layer over a substrate
242
Anneal the porous semiconductor layer
244
Form a crystalline epitaxial layer over the porous semiconductor layer
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

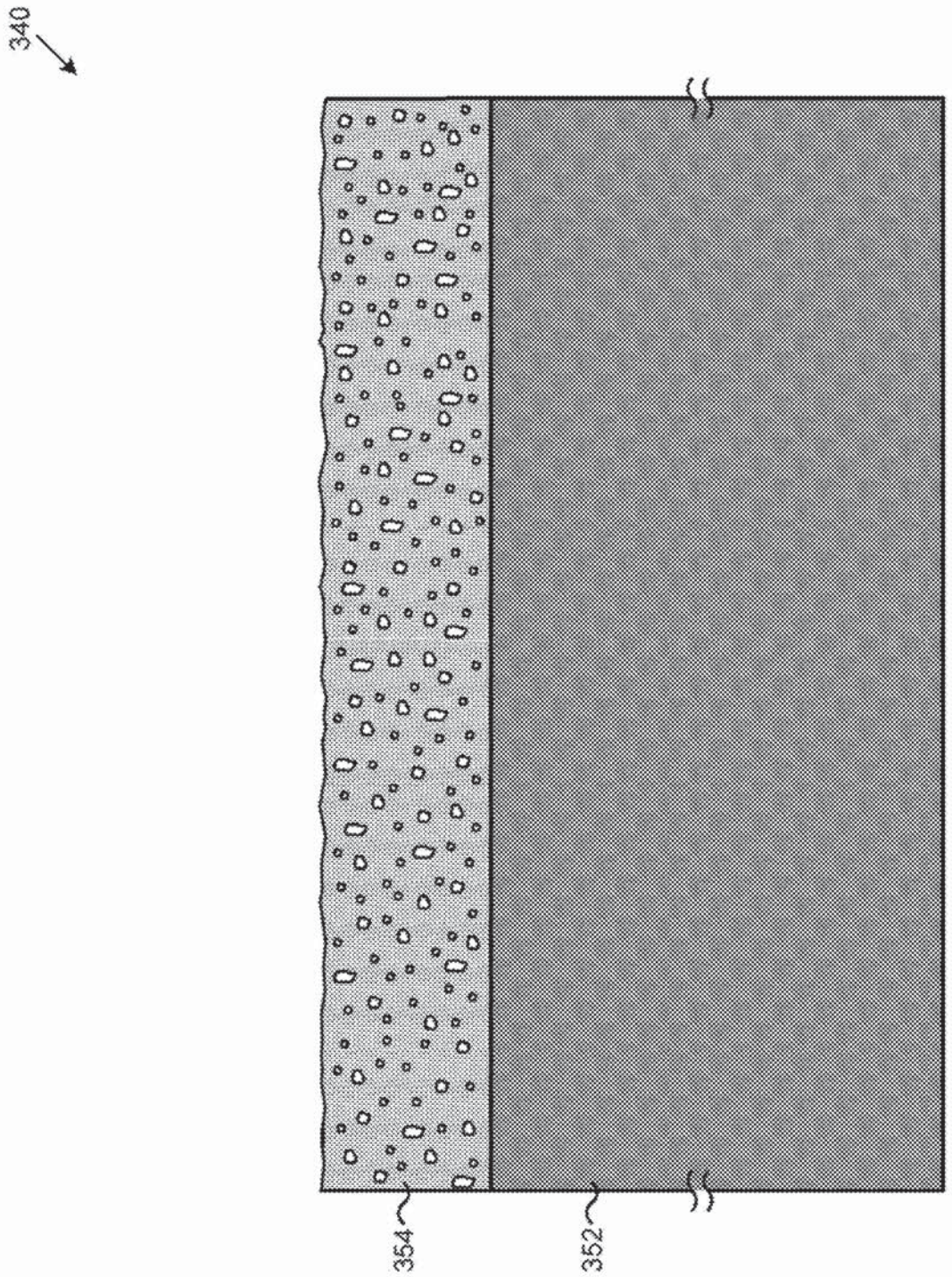


FIG. 3A

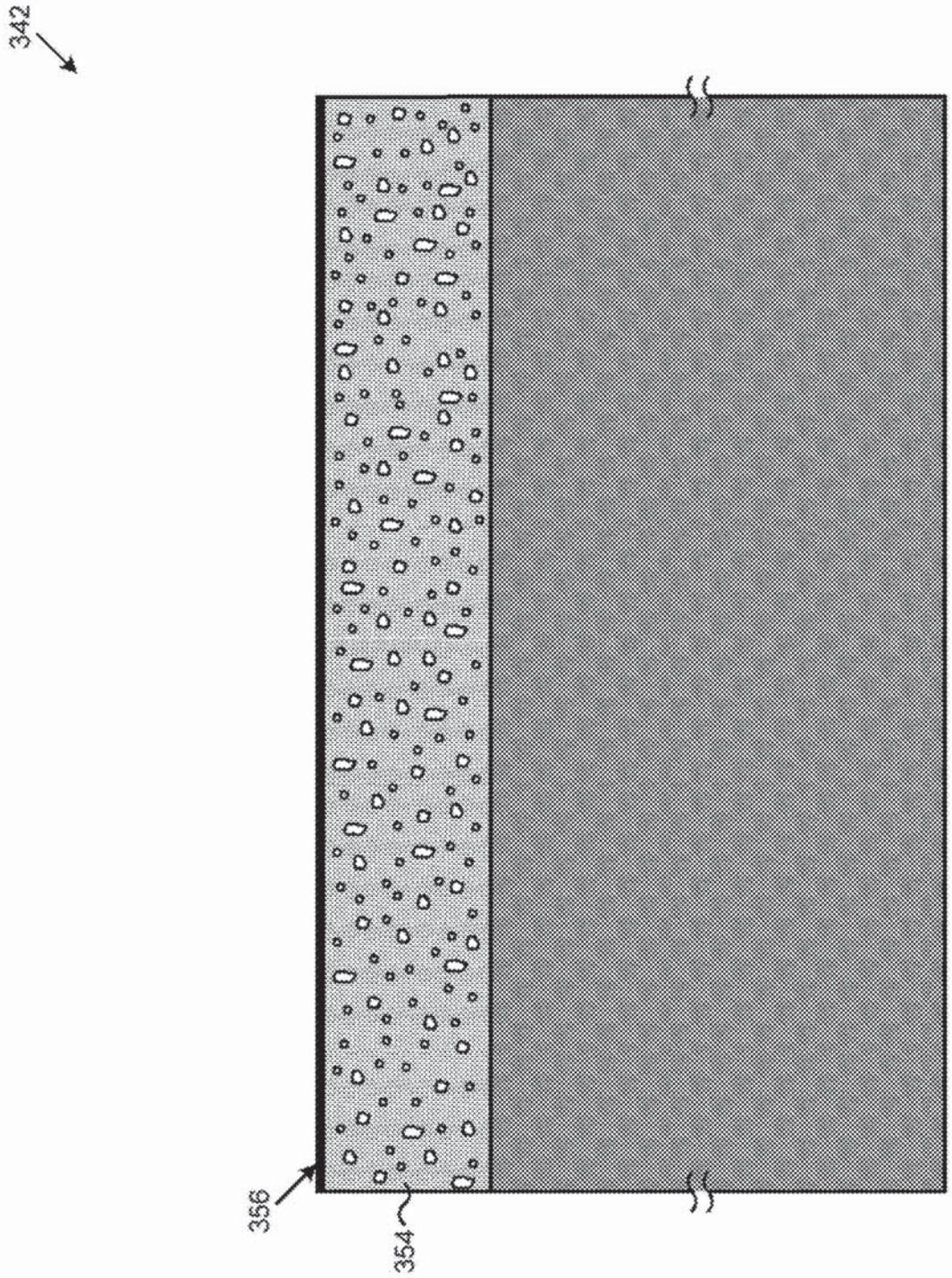


FIG. 3B

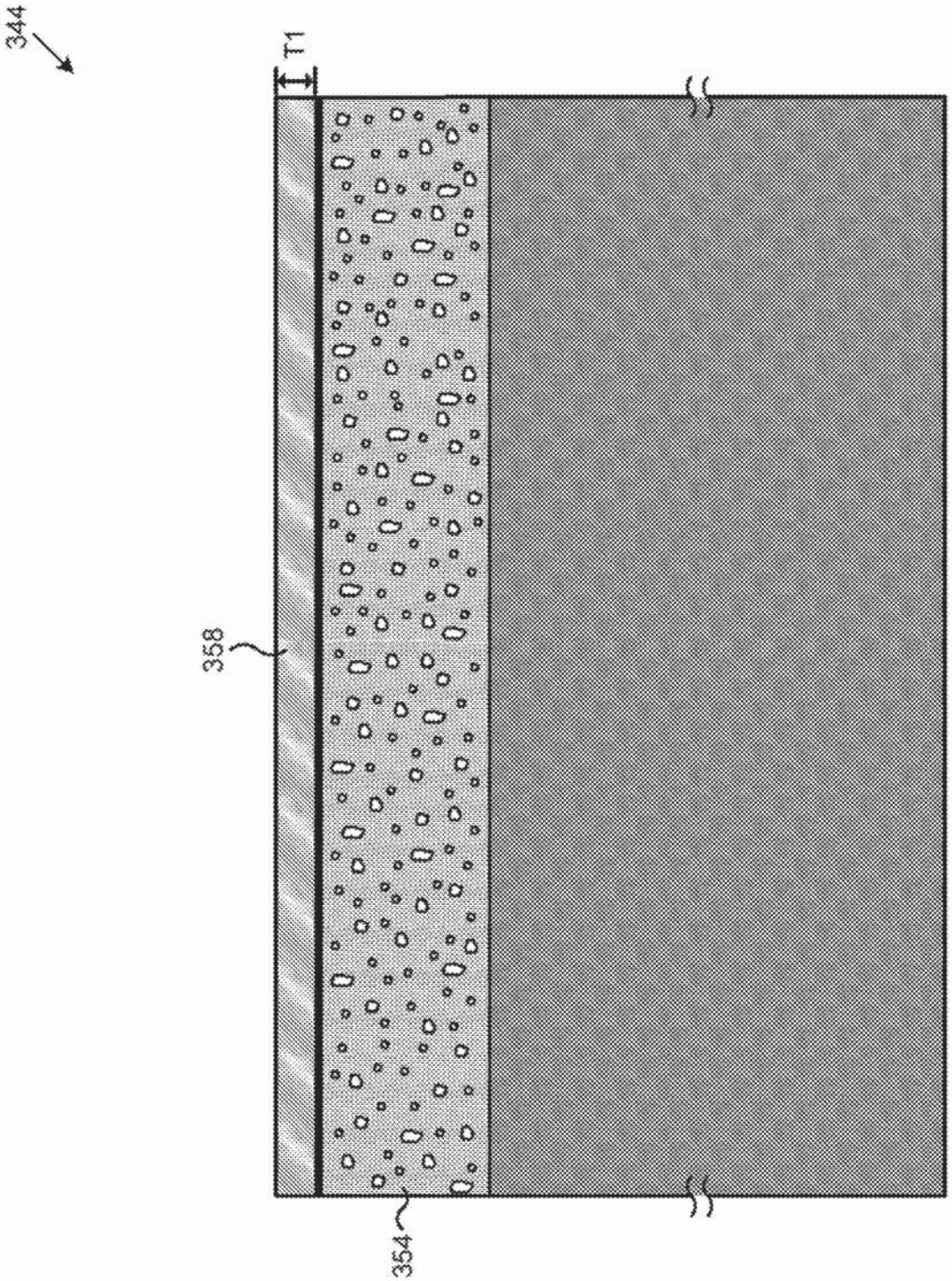


FIG. 3C

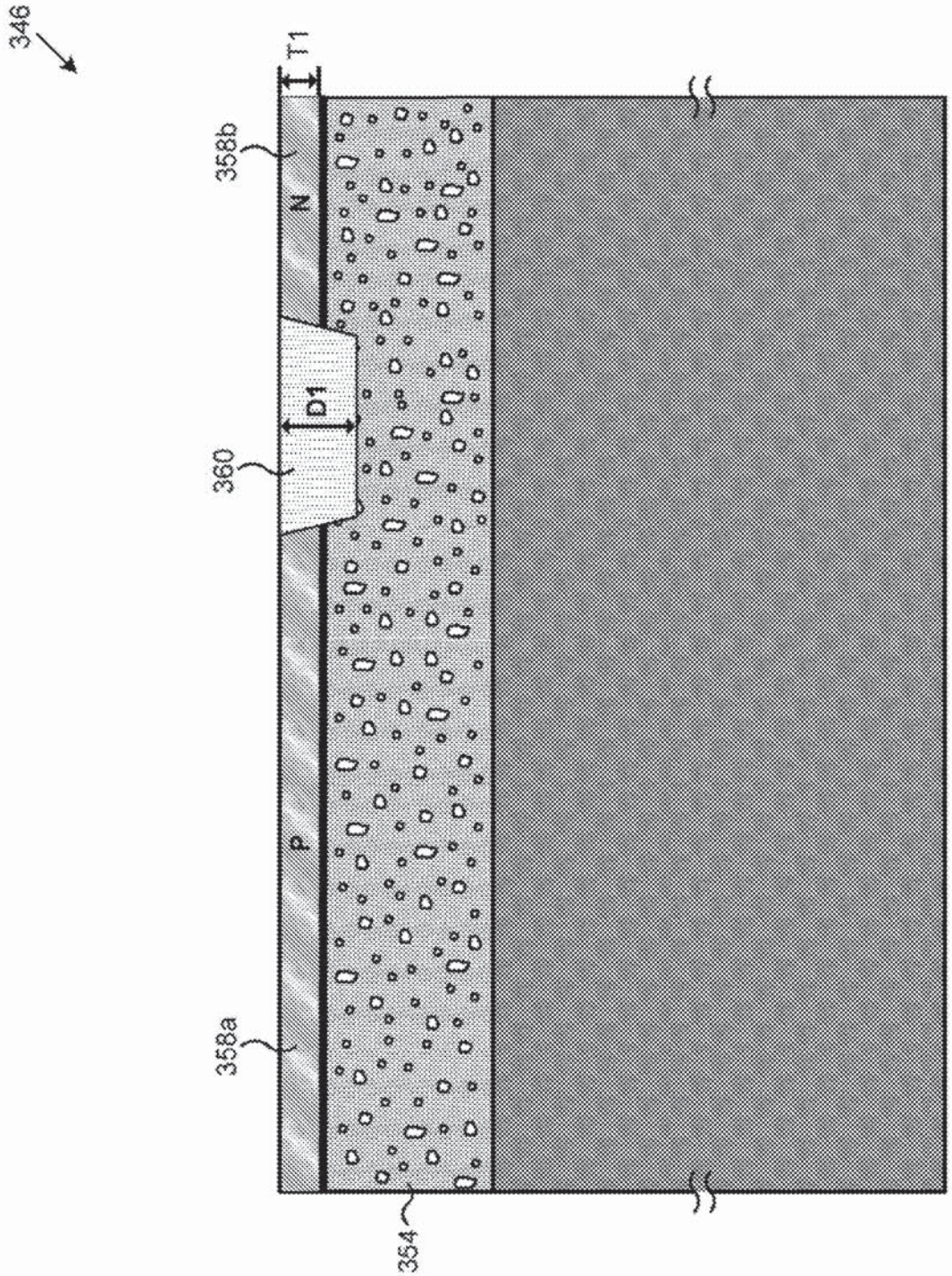
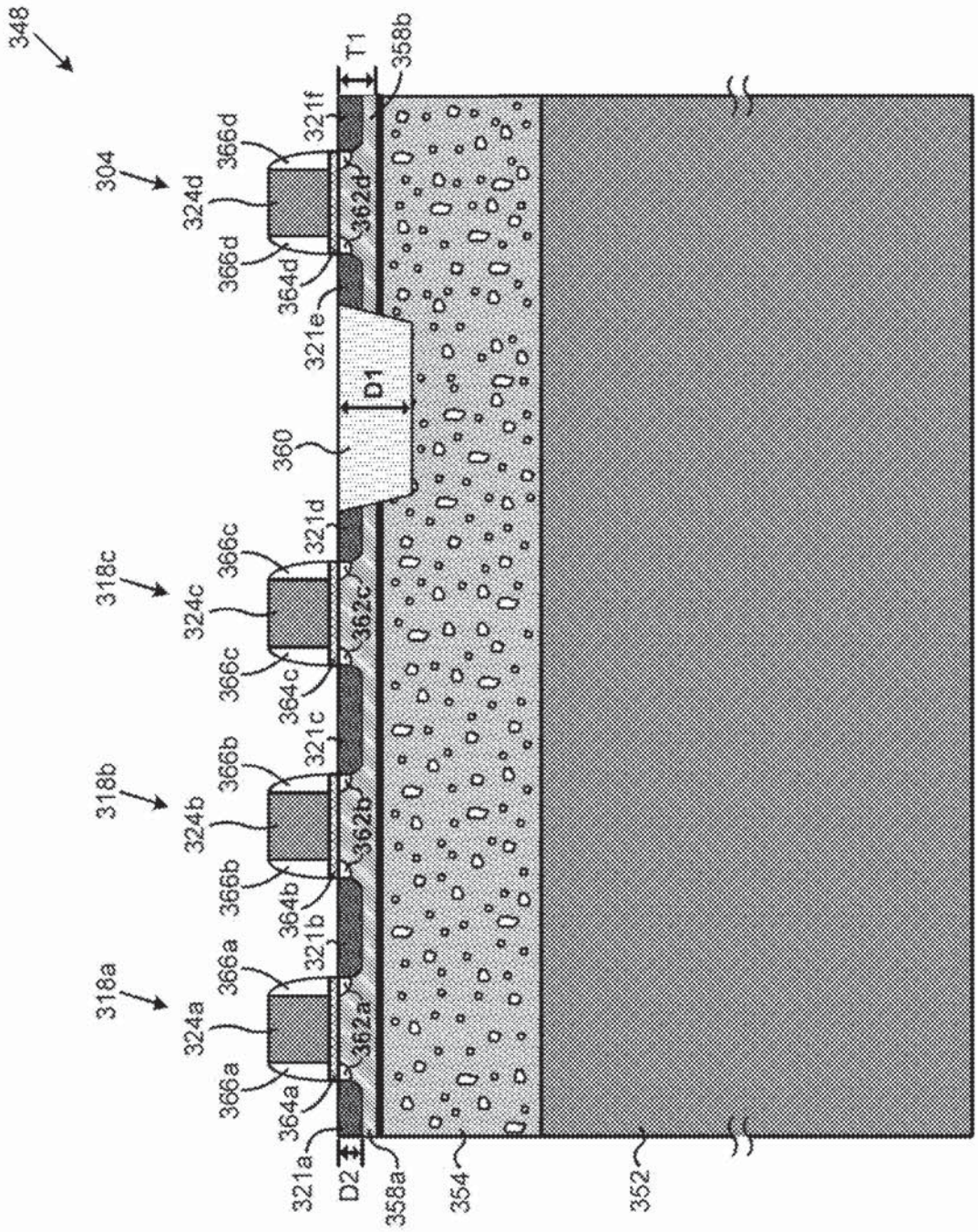


FIG. 3D


348
304
318a
318b
318c
324a
324b
324c
324d
366a
366b
366c
366d
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364b
364c
364d
362a
362b
362c
362d
321a
321b
321c
321d
321e
321f
D1
D2
T1
360
358a
358b
354
352

FIG. 3E

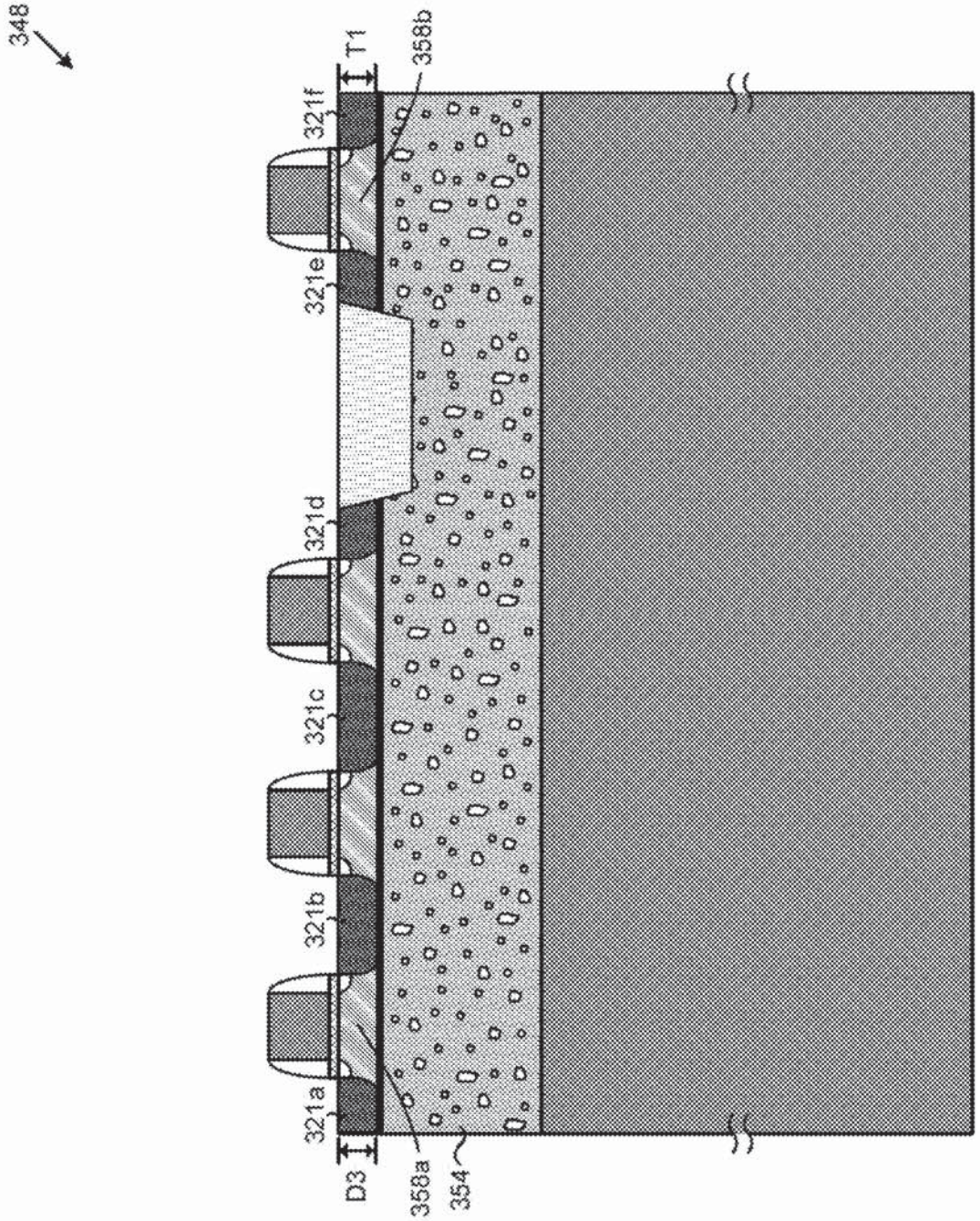

FIG. 3F

SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR LAYER FOR RF DEVICES

BACKGROUND

Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

As known in the art, a handle wafer finctioning as a substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

Thus, there is need in the art for efficiently and effectively fabricating RF devices with reduced signal leakage at low cost while overcoming the disadvantages and deficiencies of the previously known approaches.

SUMMARY

The present disclosure is directed to a semiconductor structure having porous semiconductor layer for RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between RF switch **112** and LNA **108**. Receive output **106** receives amplified RF signals from LNA **108**. In one implementation, receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor **126***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to LNA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

In the present implementation, transistors **118***a*, **118***b*, **1/8***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FETs (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF state voltage handling capability of forty volts (40 V). In various implementations. RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

As described below, in conventional semiconductor structures, signals can leak from RF switch **112**, for example, to ground or to other devices. This signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency signals, such as RF signals. According to the present application, RF switch **112** can be utilized in a semiconductor structure that reduces signal leakage. It is noted that, although the present application focuses on RF signals, the signals may have frequencies other than RF frequencies.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown in FIG. **3**A, according to action **240**, semiconductor structure **340** including porous semiconductor layer **354** situated over substrate **352** is formed. In the present implementation, substrate **352** is a bulk silicon substrate. For example, substrate **352** can be a P-type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, substrate **352** may be any other type of substrate.

Porous semiconductor layer **354** situated over substrate **352** is a semiconductor layer having voids, or pores, therein. Within porous semiconductor layer **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous semiconductor layer **354** can be formed by using a top-down technique, where portions of substrate **352** are removed to generate pores. For example, porous semiconductor layer **354** can be formed by electrochemical etching using hydrofluoric acid (HF). Alternatively, porous semiconductor layer **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art. Porous semiconductor layer **354** can also be formed by using a bottom-up technique, where deposition results in a semiconductor layer having empty spaces. For example, porous semiconductor layer **354** can be formed by low-temperature high-density plasma (HDP) deposition. Alternatively, porous semiconductor layer **354** can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous semiconductor layer **354** is a porous silicon layer, and has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous semiconductor layer **354** may be any other type of porous semiconductor layer.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous semiconductor layer **354** is annealed. For example, porous semiconductor layer **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous semiconductor layer **354** into larger cavities, while closing and smoothing surface **356** of porous semiconductor layer **354**. The annealed porous semiconductor layer **354** serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous semiconductor layer **354**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material situated over porous semiconductor layer **354**. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known in the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and

has thickness T1 from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation region **360** is formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358** and into porous semiconductor layer **354**.

Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358** and into porous semiconductor layer **354**, then depositing an electrically insulating material. In the present implementation, electrical isolation region **360** is also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using chemical machine polishing (CMP). Electrical isolation region **360** can comprise, for example, silicon dioxide (SiO_2).

In the present implementation, depth D1 of electrical isolation region **360** is greater than thickness T1 of crystalline epitaxial layer **358**. Accordingly, electrical isolation region **360** separates crystalline epitaxial layer **358** of FIG. **3**C into two crystalline epitaxial layers **358***a* and **358***b*. In one implementation, depth D1 of electrical isolation region **360** can be substantially equal to thickness T1. In another implementation, depth D1 of electrical isolation region **360** can be less than thickness T1, such that electrical isolation region **360** extends into crystalline epitaxial layer **358** but not into porous semiconductor layer **354**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation region **360**.

Crystalline epitaxial layers **358***a* and **358***b* can also be implanted with a dopant. For example, crystalline epitaxial layers **358***a* and **358***b* can be implanted with boron or other appropriate P-type dopant. In another example, one or both of crystalline epitaxial layers **358***a* and **358***b* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a* and **358***b* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a* and **358***b* are implanted with a dopant after forming electrical isolation region **360**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation region **360**. In this implementation, electrical isolation region **360** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

As described below, electrical isolation region **360** reduces signal interference across crystalline epitaxial layers **358***a* and **358***b*. Electrical isolation region **360** is considered optional in that semiconductor structures according to the present application can be formed without electrical isolation region **360**.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. **3**E, semiconductor devices **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, semiconductor device **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates semiconductor device **304** from semiconductor devices **318***a*, **318***b*, and **318***c*.

In the present implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors. Semiconductor devices **318***a*, **318***b*, and **318***c* in FIG. **3**E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Semiconductor device **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Semiconductor device **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Semiconductor device **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

In the present implementation, semiconductor device **304** is also a transistor. Semiconductor device **304** in FIG. **3**E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Semiconductor device **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*.

In one implementation, semiconductor device **304** can be utilized as part of a logic circuit. Semiconductor device **304** is considered optional in that semiconductor structures according to the present application can be formed without semiconductor device **304**.

Gates **324***a*, **324***b*, **324***c*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

In the present implementation, depth D2 of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T1 of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous semiconductor layer **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) in another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* and/or gates **324***a*, **324***b*, and **324***c*. In various implementations, semiconductor structure **348** can include more or fewer semiconductor devices in crystalline epitaxial layer **358***a*. In various implementations, crystalline epitaxial layers **358***a* and **358***b* can include diodes, or types of semiconductor devices instead of or in addition to transistors.

Because semiconductor structure **348** includes porous semiconductor layer **354** (for example, a porous silicon layer), semiconductor structure **348** reduces signal leakage (for example, RF signal leakage) from semiconductor devices **318***a*, **318***b*, **318***c*, and **304** to ground. Further, porous semiconductor layer **354** (for example, a porous silicon layer) reduces signal interference (for example, RF signal interference) between the different devices built in crystalline epitaxial layers **358***a* and **358***b*. Pores in porous semiconductor layer **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. **3**E, porous semiconductor layer **354** has a dielectric constant substantially less than the dielectric constant of substrate **352**. For example, when substrate **352** is a bulk silicon substrate having a dielectric constant of approximately 11.7, porous semiconductor layer **354** has a dielectric constant significantly less than 11.7. In particular, porous semiconductor layer **354** can have a dielectric constant from approximately 2.0 to approximately 4.0. The improved RF isolation that results from the low dielectric constant is especially advantageous for RF switching applications as it reduces signal distortion (i.e. improves linearity). It also results in a more uniform voltage distribution across the OFF state FET stack, increasing its power handling capability.

In semiconductor structure **348** in FIG. **3**E, utilizing porous semiconductor layer **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and substrate **352**. Accordingly, RF signals are less likely to leak from semiconductor devices **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to substrate **352**. For example, in one implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*, while the RF signals would have been subject to adverse impact of parasitic capacitances with substrate **352** if porous semiconductor layer **354** were not utilized. In other words, the RF signals could easily leak from semiconductor devices **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous semiconductor layer **354**, could also result in a higher insertion loss.

Because semiconductor structure **348** includes porous semiconductor layer **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces signal interference from semiconductor devices **318***a*, **318***b*, **318***c* to semiconductor device **304**, and vice versa. If porous semiconductor layer **354** and electrical isolation region **360** were not utilized, signals (for example RF signals) from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or substrate **352**, and interfere with semiconductor devices **318***a*, **318***b*, **318***c* and generate additional undesirable noise in semiconductor devices **318***a*, **318***b*, **318***c*. Where semiconductor device **304** is a transistor utilized in PA **104** (shown in FIG. **1**), these consequences could be amplified. Together, the low dielectric constant of porous semiconductor layer **354** and electrical insulation of electrical isolation region **360** reduce signal leakage and interference through crystalline epitaxial layers **358***a* and **358***b* and/or substrate **352**. The leakage and interference are especially reduced where depth D**1** of electrical isolation region **360** is equal to or greater than thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*.

Semiconductor structure **348** in FIG. **3**E can achieve this reduced signal leakage without using costly materials for substrate **352**, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above porous semiconductor layer **354** (for example, a porous silicon layer) can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous semiconductor layer **354** (for example, a porous silicon layer) can be situated over bulk semiconductor substrate **352** (for example, a bulk silicon substrate), and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous semiconductor layer **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which semiconductor devices **318***a*, **318***b*, **318***c*, and **304** are formed. Further, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of semiconductor devices **318***a*, **318***b*, and **318***c* by reducing junction capacitances.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D**3** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are in contact with porous semiconductor layer **354**. Compared to semiconductor structure **348** of FIG. **3**E, deeper source/drain junctions **321***e* and **321***f* in semiconductor structure **348** of FIG. **3**F improve performance of semiconductor device **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

The invention claimed is:

1. A semiconductor structure comprising:

a substrate having a first dielectric constant;

a porous semiconductor layer situated over said substrate;

at least one crystalline epitaxial layer situated directly on said porous semiconductor layer;

a first semiconductor device situated in said at least one crystalline epitaxial layer;

said porous semiconductor layer having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device.

2. The semiconductor structure of claim **1**, further comprising:

a second semiconductor device situated in said at least one crystalline epitaxial layer; and

an electrical isolation region separating said first and second semiconductor devices.

3. The semiconductor structure of claim **2**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

4. The semiconductor structure of claim **1**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

5. The semiconductor structure of claim **4**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

6. The semiconductor structure of claim **4**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor layer.

7. The semiconductor structure of claim **1**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a semiconductor material selected from one of said first semiconductor material and a second semiconductor material.

8. A semiconductor structure comprising:

a porous silicon layer;

at least one crystalline epitaxial layer situated directly on said porous silicon layer;

first and second transistors situated in said at least one crystalline epitaxial layer;

an electrical isolation region separating said first and second transistors.

9. The semiconductor structure of claim **8**, wherein said porous silicon layer is situated over a bulk silicon substrate.

10. The semiconductor structure of claim **8**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

11. The semiconductor structure of claim **8**, wherein said first transistor is utilized in a radio frequency (RF) switch.

12. The semiconductor structure of claim **8**, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon layer.

13. The semiconductor structure of claim **8**, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon layer.

14. A semiconductor structure comprising:

a porous semiconductor layer situated over a substrate, said porous semiconductor layer having a higher resistivity than said substrate;

at least one crystalline epitaxial layer situated directly on said porous semiconductor layer;

a first semiconductor device situated in said at least one crystalline epitaxial layer.

15. The semiconductor structure of claim **14**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material.

16. The semiconductor structure of claim **14**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a second semiconductor material.

17. The semiconductor structure of claim **14**, further comprising:

a second semiconductor device situated in said at least one crystalline epitaxial layer; and

an electrical isolation region separating said first and second semiconductor devices.

18. The semiconductor structure of claim **17**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

19. The semiconductor structure of claim **14**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

20. The semiconductor structure of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

* * * * *

Exhibit 3

US011195920B2

(12) **United States Patent**
Hurwitz et al.

(10) **Patent No.: US 11,195,920 B2**
(45) **Date of Patent: Dec. 7, 2021**

(54) **SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR SEGMENT FOR RF DEVICES AND BULK SEMICONDUCTOR REGION FOR NON-RF DEVICES**

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(72) Inventors: **Paul D. Hurwitz**, Irvine, CA (US); **Edward Preisler**, San Clemente, CA (US); **David J. Howard**, Irvine, CA (US); **Marco Racanelli**, Santa Ana, CA (US)

(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/598,803**

(22) Filed: **Oct. 10, 2019**

(65) **Prior Publication Data**

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Related U.S. Application Data

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H01L 29/10 (2006.01)
H01L 23/66 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/1083*** (2013.01); ***H01L 21/02428*** (2013.01); ***H01L 21/324*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC ... H01L 29/1083; H01L 23/66; H01L 21/324; H01L 21/02428; H01L 27/088; H01L 29/10; H01L 21/02; H01L 21/02532; H01L 21/02667; H01L 21/76224; H01L 2223/6688
(Continued)

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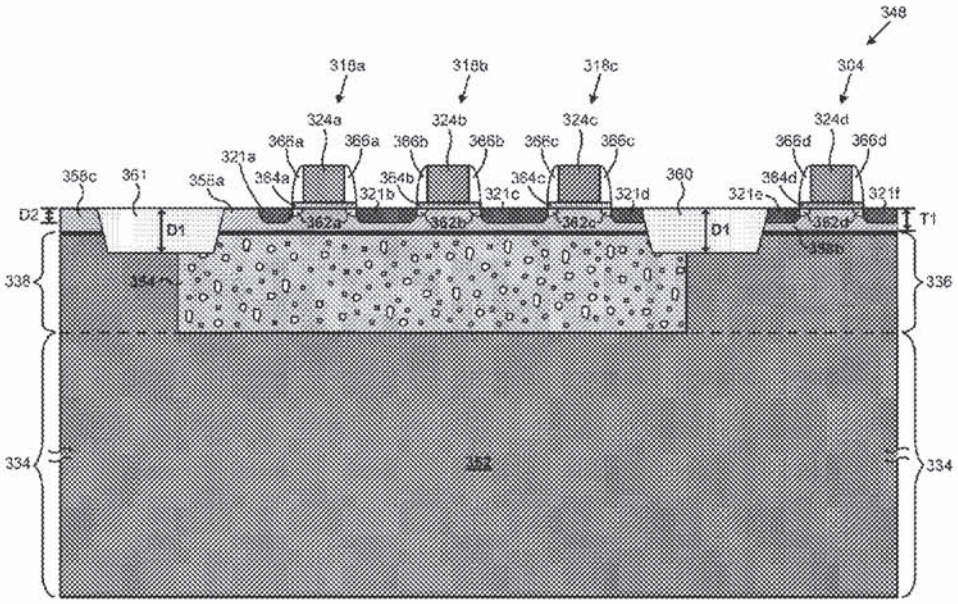
Primary Examiner — Alexander O Williams
(74) *Attorney, Agent, or Firm* — Farjami & Farjami LLP

(57) **ABSTRACT**

A semiconductor structure includes a porous semiconductor segment adjacent to a first region of a substrate, and a crystalline epitaxial layer situated over the porous semiconductor segment and over the first region of the substrate. A first semiconductor device is situated in the crystalline epitaxial layer over the porous semiconductor segment. The first region of the substrate has a first dielectric constant, and the porous semiconductor segment has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor segment reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer over the first region of the substrate, and an electrical isolation region separating the first and second semiconductor devices.

19 Claims, 8 Drawing Sheets



(51) **Int. Cl.**
H01L 21/324 (2006.01)
H01L 27/088 (2006.01)
H01L 21/02 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/66*** (2013.01); ***H01L 27/088*** (2013.01); *H01L 2223/6688* (2013.01)

(58) **Field of Classification Search**
USPC 257/347
See application file for complete search history.

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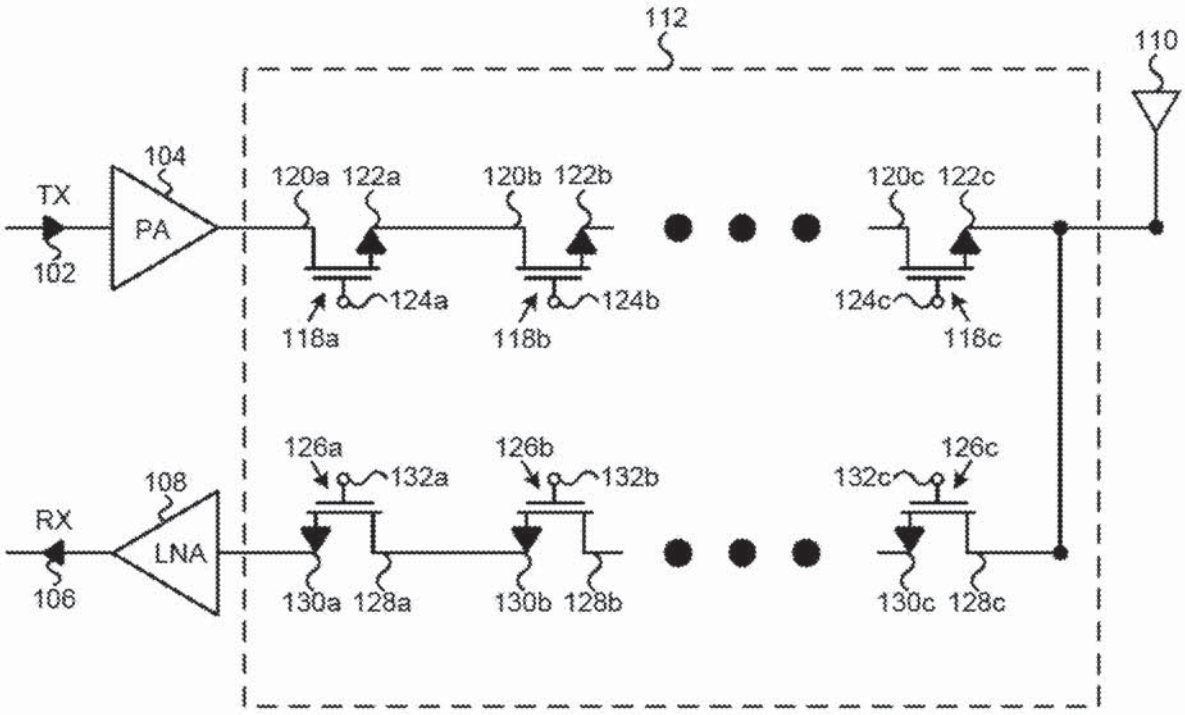
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110
104
TX
PA
102
120a 122a
120b 122b
120c 122c
124a
124b
124c
118a
118b
118c
126a
126b
126c
132a
132b
132c
108
RX
LNA
106
130a 128a
130b 128b
130c 128c

FIG. 1

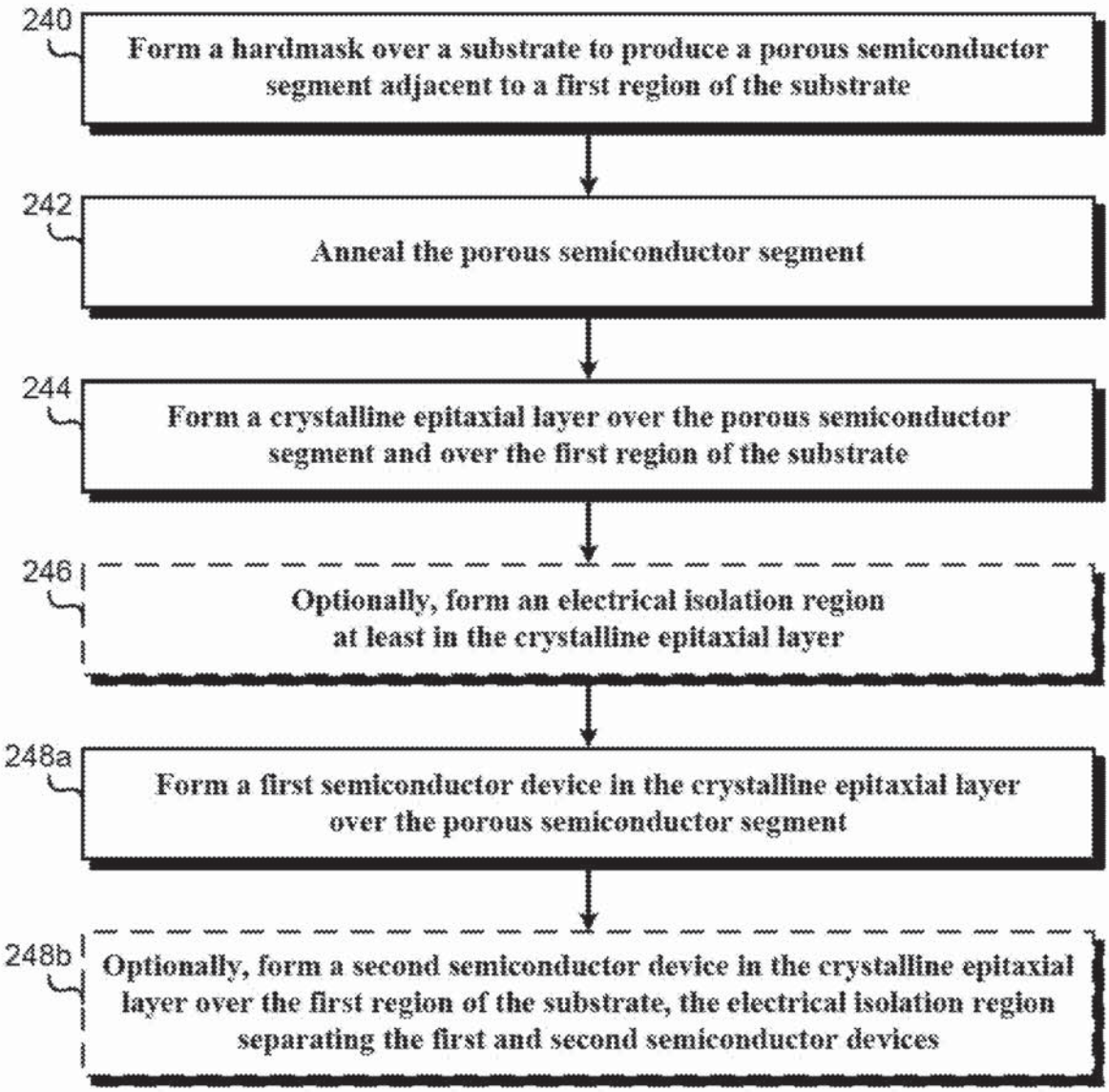

240
Form a hardmask over a substrate to produce a porous semiconductor segment adjacent to a first region of the substrate
242
Anneal the porous semiconductor segment
244
Form a crystalline epitaxial layer over the porous semiconductor segment and over the first region of the substrate
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer over the porous semiconductor segment
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer over the first region of the substrate, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

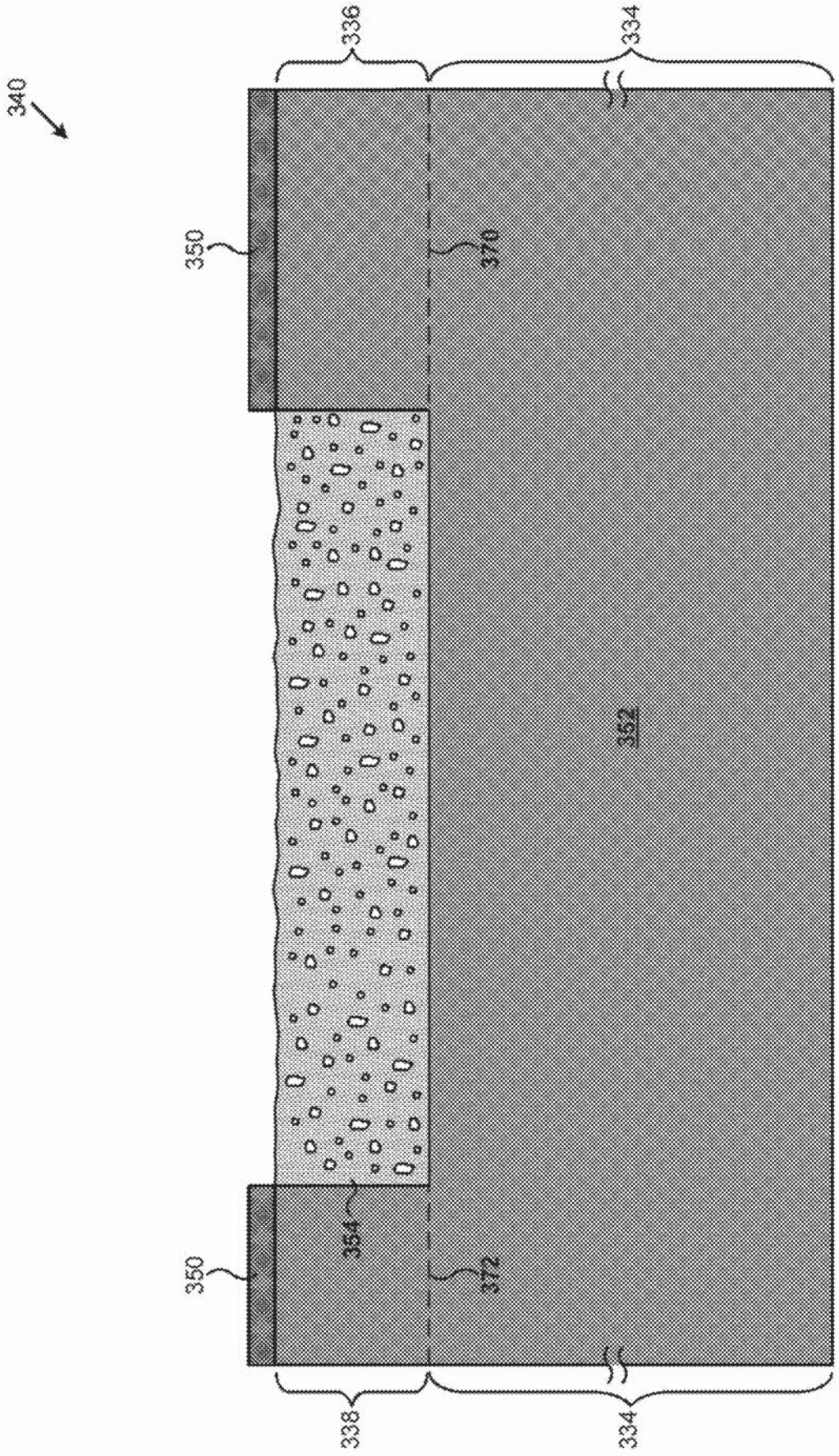


FIG. 3A

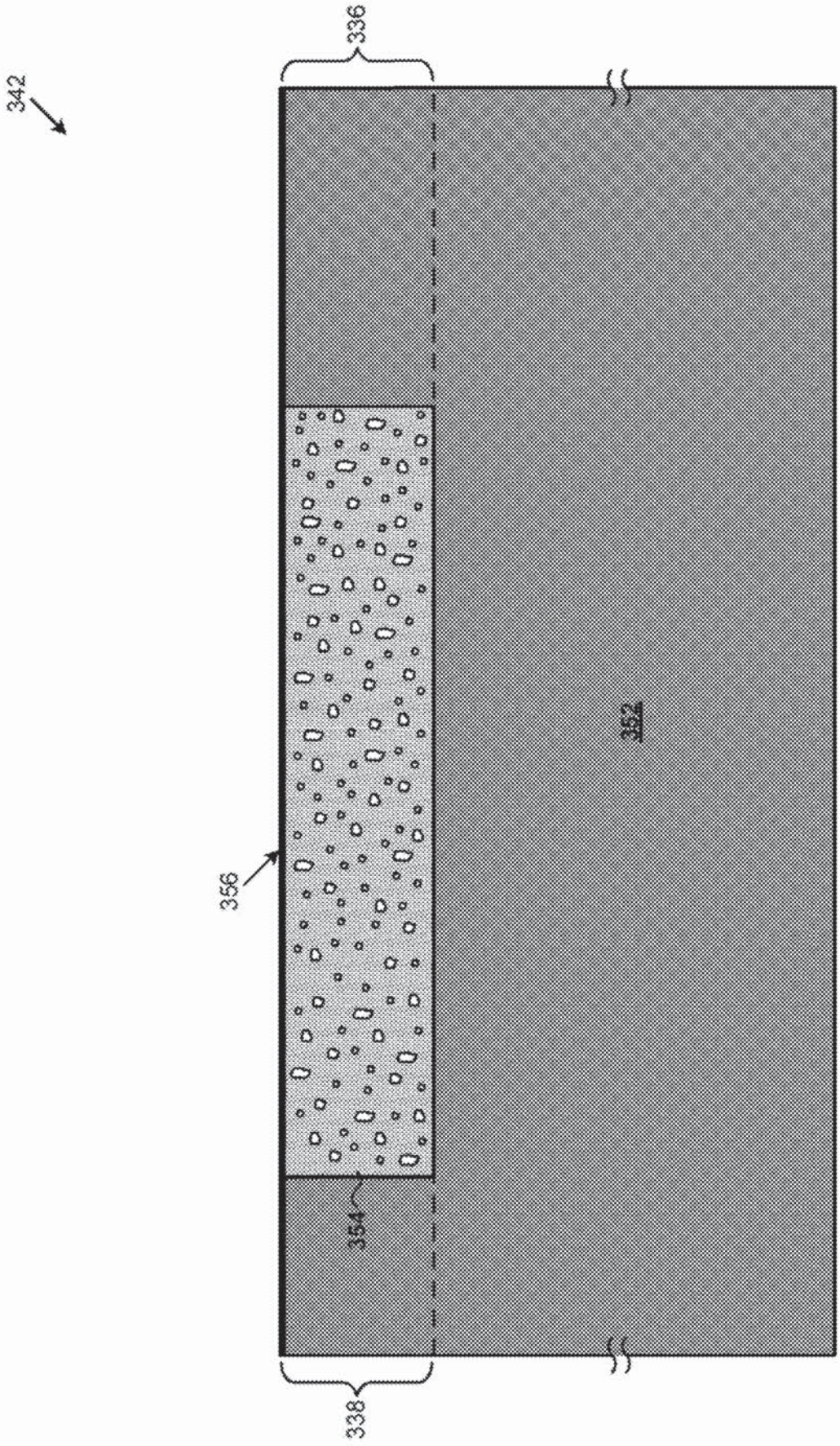


FIG. 3B

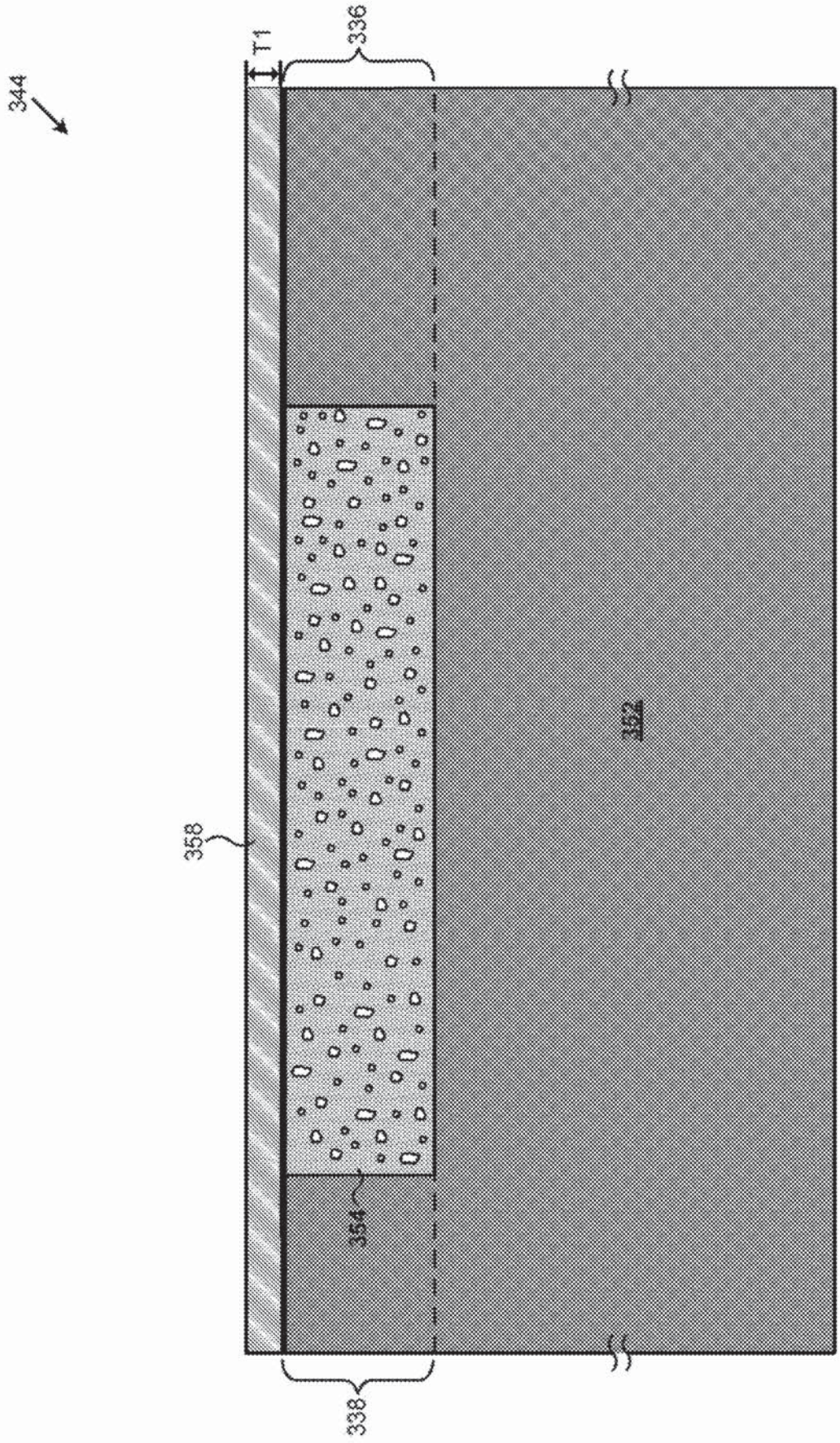


FIG. 3C

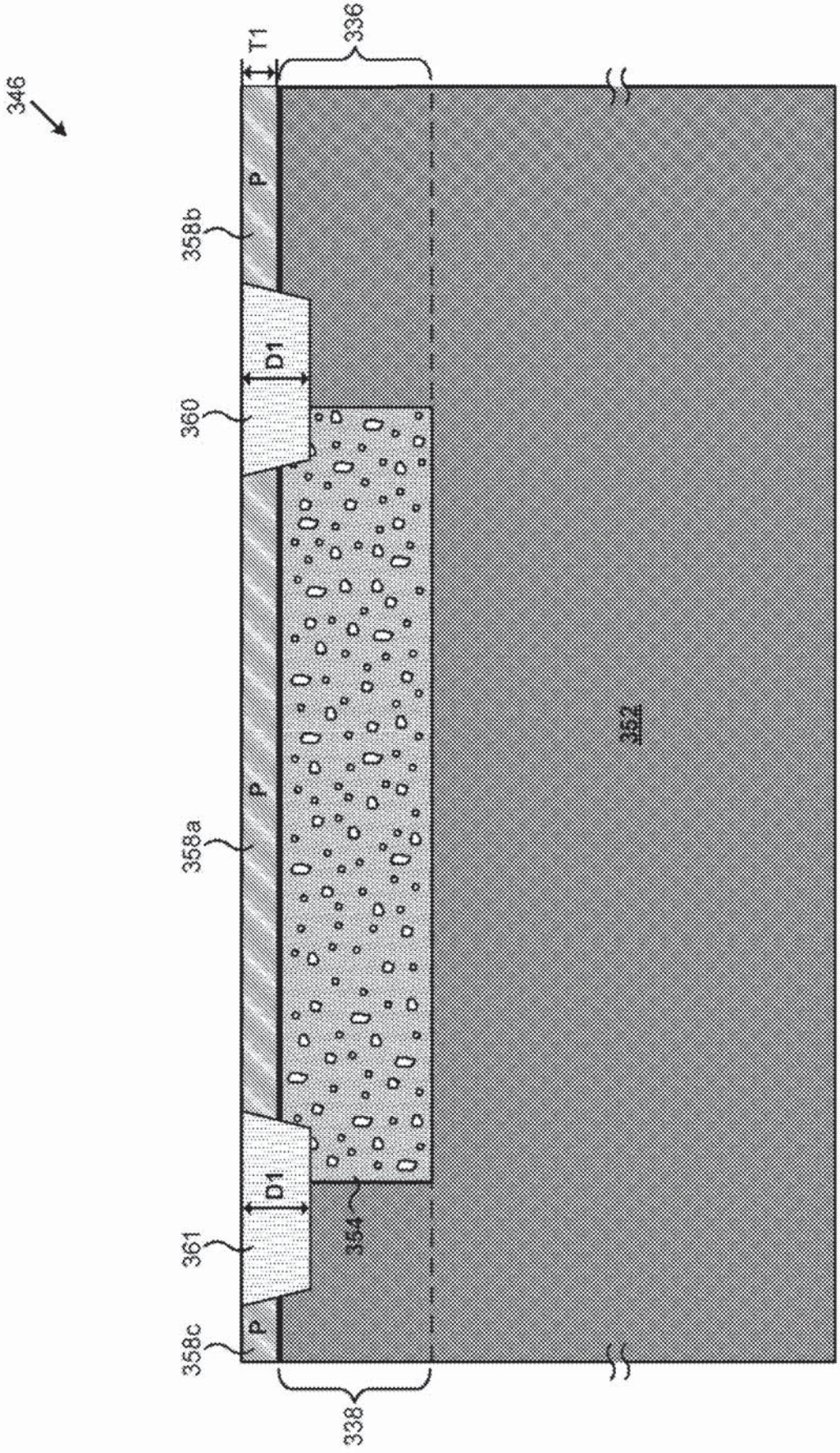
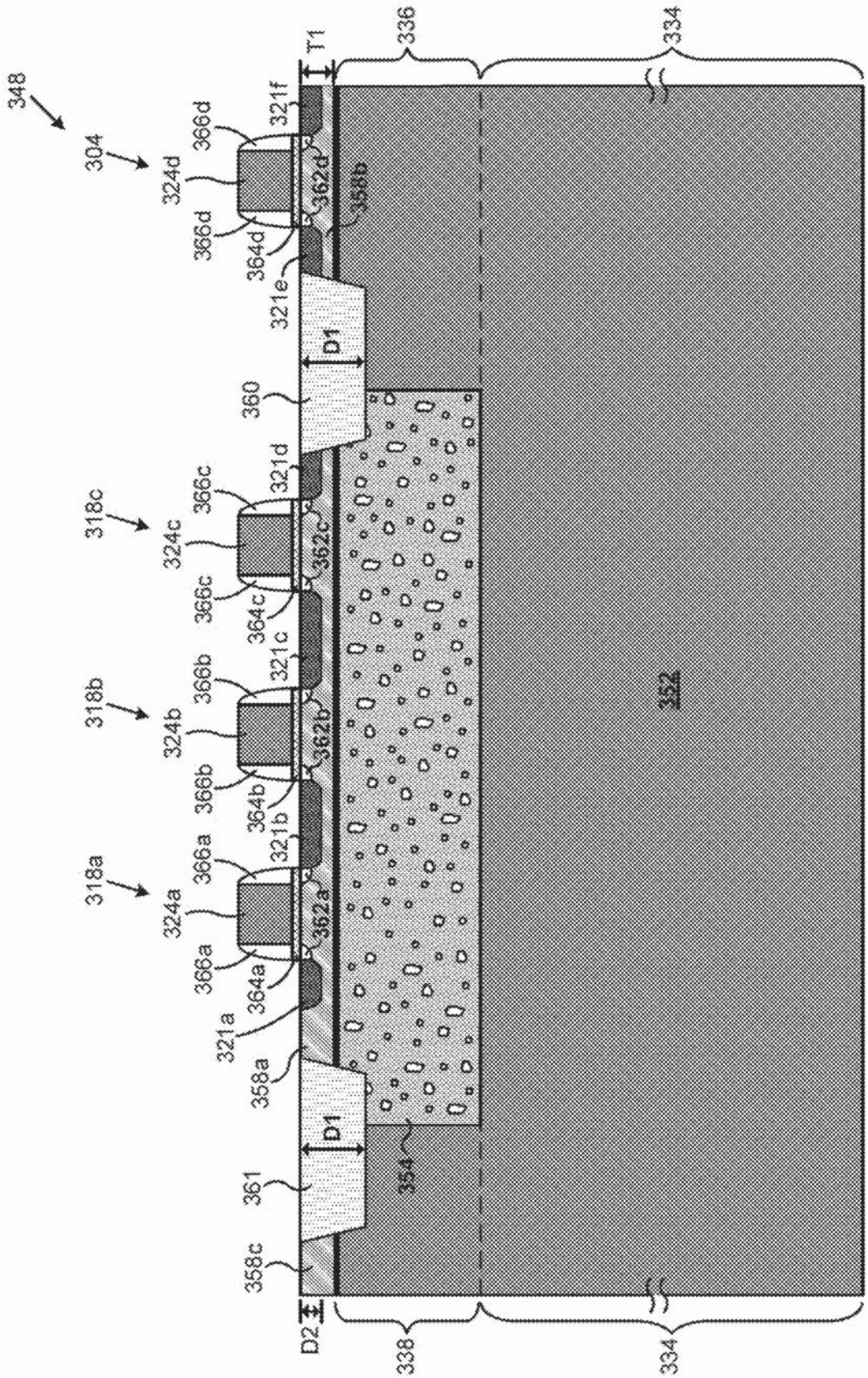


FIG. 3D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304
318a
318b
318c
324a
324b
324c
324d
366a
366b
366c
366d
364a
364b
364c
364d
362a
362b
362c
362d
321a
321b
321c
321d
321e
321f
358a
358b
358c
360
361
354
352
T1
D1
D1
D2
336
334
338
334

FIG. 3E

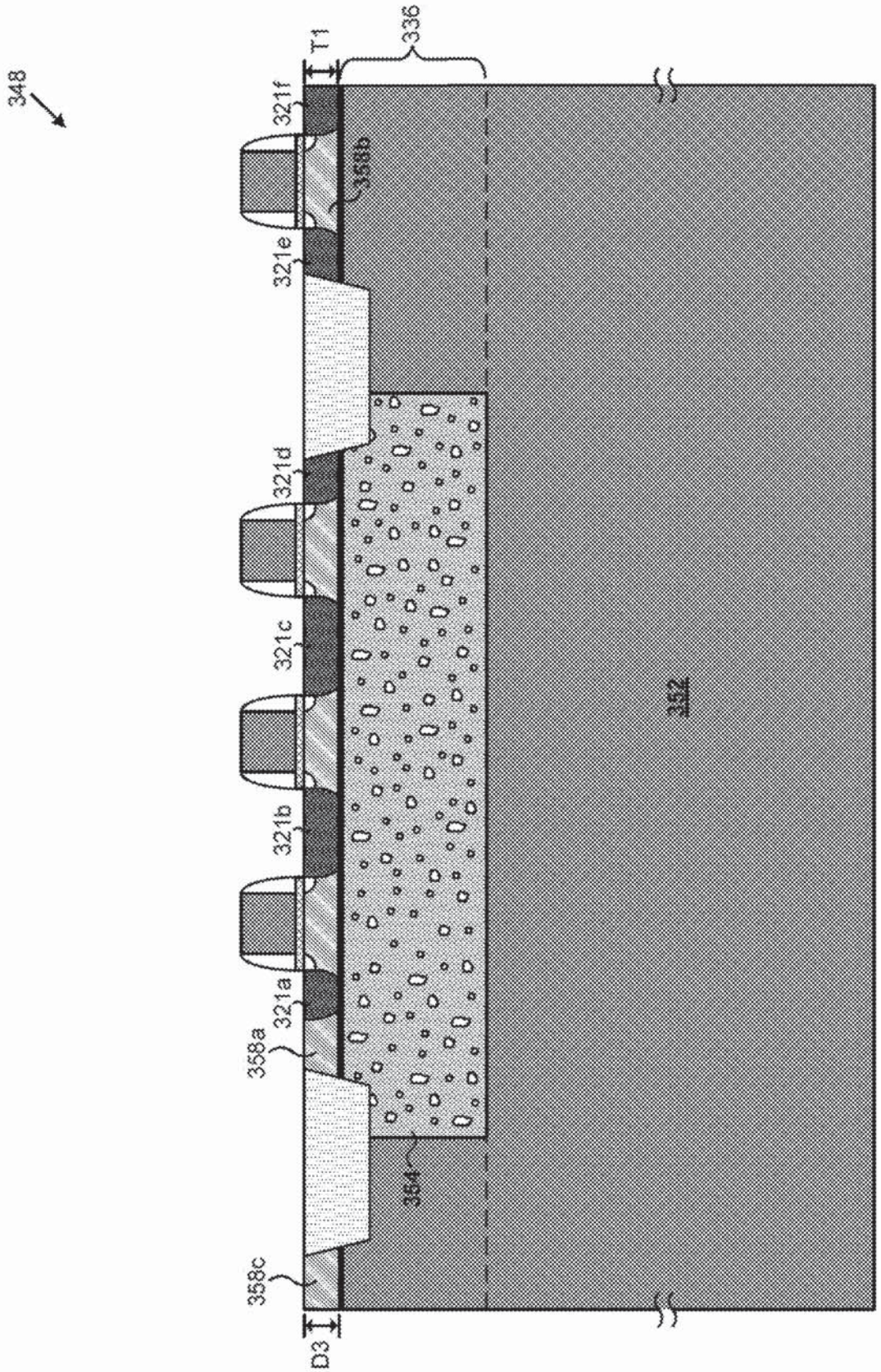
348
T1
336
321f
358b
321e
321d
321c
321b
321a
358a
364
358c
D3
352

FIG. 3F

SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR SEGMENT FOR RF DEVICES AND BULK SEMICONDUCTOR REGION FOR NON-RF DEVICES

CLAIMS OF PRIORITY

The present application is a continuation-in-part of and claims the benefit of and priority to application Ser. No. 16/597,779 filed on Oct. 9, 2019 and titled "Semiconductor Structure Having Porous Semiconductor Layer for RF Devices,". The disclosure and content of the above-identified application are hereby incorporated fully by reference into the present application.

BACKGROUND

Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

As known in the art, a handle wafer functioning as a substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

Further, due to existence of the BOX in SOI structures, each CMOS device built in the top device layer is dielectrically isolated from the substrate. To control the body potential (avoid floating body effects, and hysteresis) each device requires its own body contact. This approach results in the consumption of much of the surface area in a die, decreasing logic density in the die. Further, the BOX has much low thermal conductivity compared to monocrystalline silicon (approximately one and half watts per meter-kelvin (1.5 W/(m·K)) versus approximately one hundred and fifty watts per meter-kelvin (150 W/(m·K)) respectively). As a result, high power components, such as power amplifiers, integrated in SOI structures cannot effectively dissipate heat.

Thus, there is need in the art for efficiently and effectively fabricating semiconductor dies with reduced RF signal leakage, reduced need for numerous body contacts, and increased heat dissipation at low cost.

SUMMARY

The present disclosure is directed to a semiconductor structure having at least one porous semiconductor segment for radio frequency (RF) devices and at least one bulk semiconductor region for non-RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

FIG. **1** illustrates a portion of a radio front-end of a transceiver (hereinafter referred to simply as a "transceiver") including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between RF switch **112** and LNA **108**. Receive output **106** receives amplified RF signals from LNA **108**. In one implementation,

receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor **126***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to LNA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

In the present implementation, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FETs (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF-state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF-state voltage handling capability of forty volts (40 V). In various implementations. RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

As described above, in conventional semiconductor structures, RF signals can leak from RF switch **112**, for example, to ground or to other devices. This RF signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency RF signals. According to the present application, RF switch **112** can be utilized in a semiconductor structure that reduces RF signal leakage. It is noted that, although the present application focuses on RF signals, the signals may have frequencies other than RF frequencies.

As also described above, conventional semiconductor structures cannot easily accommodate body contacts without tradeoffs, and cannot effectively dissipate heat from high power devices, such as PA **104**, integrated with RF switch **112**. According to the present application. RF switch **112** can be utilized in a semiconductor structure that integrates PA **104** (and/or LNA **108**) while easily accommodating body contacts and providing effective heat dissipation therefor.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown in FIG. **3**A, according to action **240**, semiconductor structure **340** includes hardmask **350** formed over bulk silicon substrate **352** to produce porous silicon segment **354** adjacent to regions **336** and **338** of bulk silicon substrate **352**.

Bulk silicon substrate **352** includes regions **334**, **336**, and **338**. Region **334** is situated under porous silicon segment **354** and under regions **336** and **338**. Regions **336** and **338** are adjacent to porous silicon segment **354** on respective sides. In FIG. **3**A, dashed line **370** illustrates the boundary of regions **334** and **336**, and dashed line **372** illustrates the boundary of regions **334** and **338**. It is understood that dashed lines **370** and **372** merely illustrate conceptual boundaries of regions **334**, **336**, and **338**, and that regions **334**, **336**, and **338** of bulk silicon substrate **352** is typically one continuous bulk semiconductor material. In the present implementation, bulk silicon substrate **352** is a P– or P+ type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, bulk silicon substrate **352** may be any other type of substrate.

Porous silicon segment **354** adjacent to regions **336** and **338** and situated over region **334** is a silicon segment having voids, or pores, therein. Within porous silicon segment **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous silicon segment **354** can be formed by using a top-down technique, where portions of bulk silicon substrate **352** are removed to generate pores. In the present implementation, hardmask **350** is formed over bulk silicon substrate **352** to expose a segment thereof. Then, porous silicon segment **354** is formed by electrochemical etching the exposed segment of bulk silicon substrate **352** using hydrofluoric acid (HF).

Hardmask **350** can comprise, for example, silicon nitride (SiN). Alternatively, porous silicon segment **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art.

Porous silicon segment **354** can also be formed by using a bottom-up technique, where deposition results in a silicon segment having voids. For example, a trench can be etched in bulk silicon substrate **352**. Then, a porous silicon layer can be formed by low-temperature high-density plasma (HDP) deposition. Then, porous silicon segment **354** can be formed by removing portions of the porous silicon layer outside the trench, for example, using chemical machine polishing (CMP). Alternatively, the porous silicon layer can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous silicon segment **354** has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous silicon segment **354** can have any other thickness. In various implementations, porous segment **354** may be a semiconductor material other than silicon.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous silicon segment **354** is annealed. For example, porous silicon segment **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous silicon segment **354** into larger cavities, while closing and smoothing surface **356**. The annealed porous silicon segment **354**, along with regions **336** and **338** of bulk silicon substrate **352**, serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous silicon segment **354** and over regions **336** and **338** of bulk silicon substrate **352**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known in the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and has thickness T**1** from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation regions **360** and **361** are formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **336** of bulk silicon substrate **352**. Similarly, electrical isolation region **361** extends through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **338** of bulk silicon substrate **352**.

Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **336** of bulk silicon substrate **352**, then depositing an electrically insulating material. Similarly, electrical isolation region **361** can be formed by etching through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **338** of bulk silicon substrate **352**, then depositing an electrically insulating material. In the present implementation, electrical isolation regions **360** and **361** are also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using CMP. Electrical isolation regions **360** and **361** can comprise, for example, silicon dioxide (SiO_2). In the present implementation, depth D**1** of electrical isolation regions **360** and **361** is greater than thickness T**1** of crystalline epitaxial layer **358**. Accordingly, electrical isolation regions **360** and **361** separate crystalline epitaxial layer **358** of FIG. **3**C into three crystalline epitaxial layers **358***a*, **358***b*, and **358***c*.

In one implementation, depth D**1** of electrical isolation regions **360** and **361** can be substantially equal to thickness T**1**. In another implementation, depth D**1** of electrical isolation regions **360** and **361** can be less than thickness T**1**, such that electrical isolation regions **360** and **361** extend into crystalline epitaxial layer **358**, but not into porous silicon segment **354** or regions **336** and **338** of bulk silicon substrate **352**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation regions **360** and **361**. In various implementations, electrical isolation regions **360** and **361** can extend into porous silicon segment **354**, but not into regions **336** and **338** of bulk silicon substrate **352**, or vice versa. In various implementations, semiconductor structure **346** includes additional electrical isolation regions.

Crystalline epitaxial layers **358***a*, **358***b*, and **358***c* can also be implanted with a dopant. In the present implementation, crystalline epitaxial layers **358***a*, **358***b*, and **358***c* are implanted with boron or other appropriate P-type dopant. In another implementation, one, two, or all of crystalline epitaxial layers **358***a*, **358***b*, and **358***c* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a*, **358***b*, and **358***c* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a*, **358***b*, and **358***c* are implanted with a dopant after forming electrical isolation regions **360** and **361**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation regions **360** and **361**. In this implementation, electrical isolation regions **360** and **361** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

As described below, electrical isolation regions **360** and **361** reduce RF signal interference across crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. Electrical isolation regions **360** and **361** are considered optional in that semiconductor structures according to the present application can be formed without electrical isolation regions **360** and **361**.

FIG. 3E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. 3E, transistors **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, transistor **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates transistor **304** from transistors **318***a*, **318***b*, and **318***c*.

Transistors **318***a*, **318***b*, and **318***c* in FIG. 3E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Transistor **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Transistor **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Transistor **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

Transistor **304** in FIG. 3E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Transistor **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*. In one implementation, transistor **304** can be utilized as part of a logic circuit. Transistor **304** is considered optional in that semiconductor structures according to the present application can be formed without transistor **304**.

Gates **324***a*, **324***b*, **324***c*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

In the present implementation, depth D**2** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T**1** of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous silicon segment **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) in another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* and/or gates **324***a*, **324***b*, **324***c*, and **324***d*. In various implementations, semiconductor structure **348** can include more or fewer transistors in crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. For example, another transistor (not shown) can be situated in crystalline epitaxial layer **358***c*, separated from transistors **318***a*, **318***b*, and **318***c* by electrical isolation region **361**. In various implementations, crystalline epitaxial layers **358***a*, **358***b*, **358***c* can include other types of semiconductor devices instead of or in addition to transistors **318***a*, **318***b*, **318***c*, and **304**, such as diodes.

Because semiconductor structure **348** includes porous silicon segment **354**, semiconductor structure **348** reduces RF signal leakage from transistors **318***a*, **318***b*, and **318***c* to ground. Further, porous silicon segment **354** reduces RF signal interference between the different devices built in crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. Pores in porous silicon segment **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. 3E, porous silicon segment **354** has a dielectric constant significantly less than the dielectric constant of bulk silicon substrate **352**. For example, bulk silicon substrate **352** may have a dielectric constant of approximately 11.7, and porous silicon segment **354** may have a dielectric constant significantly less than 11.7. In particular, porous silicon segment **354** can have a dielectric constant from approximately 2.0 to approximately 4.0.

In semiconductor structure **348** in FIG. 3E, utilizing porous silicon segment **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and bulk silicon substrate **352**. Accordingly, RF signals are less likely to leak from transistors **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to bulk silicon substrate **352**. For example, in one implementation, transistors **318***a*, **318***b*, and **318***c* are utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and bulk silicon substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*. In this OFF state, the RF signals would have been subject to a significant adverse impact of parasitic capacitances with bulk silicon substrate **352** if porous silicon segment **354** were not utilized. In other words, the RF signals could easily leak from transistors **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where transistors **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous silicon segment **354**, could also result in a higher insertion loss.

Because semiconductor structure **348** includes porous silicon segment **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces RF signal interference from transistor **304** to transistors **318***a*, **318***b*, **318***c*, and vice versa. If porous silicon segment **354** and electrical isolation region **360** were not utilized, RF signals from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or bulk silicon substrate **352**, and interfere with transistors **318***a*, **318***b*, **318***c* and generate additional undesirable noise in transistors **318***a*, **318***b*, **318***c*. Where transistor **304** is utilized in PA **104** (shown in FIG. **1**) in an RF transmit path, these consequences could be amplified. Similarly, porous silicon segment **354** in combination with electrical isolation region **361** reduces RF signal interference from crystalline epitaxial layer **358***c* to transistors **318***a*, **318***b*, **318***c*, and vice versa. Together, the low dielectric constant of porous silicon segment **354** and electrical insulation of electrical isolation regions **360** and **361** reduce RF signal leakage and interference through crystalline epitaxial layers **358***a*, **358***b*, and **358***c* and/or bulk silicon substrate **352**. The RF signal leakage and interference are especially reduced where depth D**1** of electrical isolation regions **360** and **361** is equal to or greater than thickness T**1** of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*.

Semiconductor structure **348** in FIG. **3**E can achieve this reduced RF signal leakage without using costly substrate materials, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above, porous silicon segment **354** can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous silicon segment **354** can be situated over region **334** of bulk silicon substrate **352**, and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous silicon segment **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which transistors **318***a*, **318***b*, **318***c*, and **304** are formed.

Because semiconductor structure **348** includes regions **336** and **338** of bulk silicon substrate **352** adjacent to porous silicon segment **354**, semiconductor structure **348** easily accommodates body contacts for transistors, such as transistor **304**. Fewer body contacts can be used in crystalline epitaxial layers **358***b* and **358***c* than in crystalline epitaxial layer **358***a*, since crystalline epitaxial layers **358***b* and **358***c* are situated over regions **336** and **338**, respectively, of bulk silicon substrate **352** having relatively low resistivity compared to porous silicon segment **354** that underlies crystalline epitaxial layer **358***a*. Accordingly, semiconductor structure **348** achieves high device density since in areas outside of RF transistor areas (i.e., outside of crystalline epitaxial layer **358***a*), fewer body contacts are needed.

Further, regions **336** and **338** of bulk silicon substrate **352** adjacent to porous silicon segment **354** increase heat dissipation from crystalline epitaxial layers **358***a* and **358***c*. As described above, in semiconductor structure **348** in FIG. **3**E, regions **336** and **338** of bulk silicon substrate **352** have a thermal conductivity much greater than a BOX in an SOI structure. For example, bulk silicon substrate **352** may have a thermal conductivity of approximately one hundred fifty watts per meter-kelvin (150 W/(m·K)), whereas the BOX may have a thermal conductivity of approximately one and a half watts per meter-kelvin (1.5 W/(m·K)). Accordingly, high power devices, such transistor **304** utilized in PA **104** (shown in FIG. **1**), can be integrated in the same semiconductor structure **348** with transistors **318***a*, **318***b*, and **318***c* without overheating, while also accommodating reduced RF signal leakage. This integration generally reduces losses when connections are ultimately formed between transistor **304** and one of transistors **318***a*, **318***b*, and **318***c*.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D3 of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T1 of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*, such that source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are in contact with porous silicon segment **354**, and such that source/drain junctions **321***e* and **321***f* are in contact with region **336** of bulk silicon substrate **352**. In semiconductor structure **348** of FIG. **3**E, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of transistors **318***a*, **318***b*, and **318***c* by reducing junction capacitances. In semiconductor structure **348** of FIG. **3**F, deeper source/drain junctions **321***e* and **321***f* improve performance of transistor **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

The invention claimed is:

1. A semiconductor structure comprising:

a porous semiconductor segment adjacent to a first region of a substrate;

at least one crystalline epitaxial layer situated over said porous semiconductor segment and over said first region of said substrate;

a first semiconductor device situated in said at least one crystalline epitaxial layer over said porous semiconductor segment;

a second semiconductor device situated in said at least one crystalline epitaxial layer over said first region of said substrate but not over said porous semiconductor segment;

said first region of said substrate having a first dielectric constant, and said porous semiconductor segment having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor segment reduces signal leakage from said first semiconductor device.

2. The semiconductor structure of claim **1**, wherein a second region of said substrate is situated under said porous semiconductor segment and under said first region of said substrate.

3. The semiconductor structure of claim **1**, further comprising:

an electrical isolation region separating said first and second semiconductor devices.

4. The semiconductor structure of claim **3**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

5. The semiconductor structure of claim **1**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

6. The semiconductor structure of claim **5**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor segment.

7. The semiconductor structure of claim **5**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor segment.

8. A semiconductor structure comprising:

a porous silicon segment adjacent to a first region of a bulk silicon substrate;

at least one crystalline epitaxial layer situated over said porous silicon segment and over said first region of said bulk silicon substrate;

a first transistor situated in said at least one crystalline epitaxial layer over said porous silicon segment;

a second transistor situated in said at least one crystalline epitaxial layer over said first region of said bulk silicon substrate but not over said porous silicon segment;

an electrical isolation region separating said first and second transistors.

9. The semiconductor structure of claim 8, wherein a second region of said bulk silicon substrate is situated under said porous silicon segment and under said first region of said bulk silicon substrate.

10. The semiconductor structure of claim 8, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

11. The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch.

12. The semiconductor structure of claim 8, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon segment.

13. The semiconductor structure of claim 8, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon segment.

14. A semiconductor structure comprising:

a porous silicon segment adjacent to a bulk silicon substrate;

at least one crystalline epitaxial layer having a first region situated over said porous silicon segment;

said at least one crystalline epitaxial layer having a second region situated over said bulk silicon substrate but not over said porous silicon segment;

an electrical isolation region separating said first region of said at least one crystalline epitaxial layer from said second region of said at least one crystalline epitaxial layer.

15. The semiconductor structure of claim 14, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

16. The semiconductor structure of claim 14, wherein a first semiconductor device is situated in said first region of said at least one crystalline epitaxial layer and a second semiconductor device is situated in said second region of said at least one crystalline epitaxial layer.

17. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor and wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon segment.

18. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor and wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon segment.

19. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor that is utilized in a radio frequency (RF) switch.

* * * * *

Exhibit 4

US011195572B2

(12) **United States Patent**
Best et al.

(10) **Patent No.: US 11,195,572 B2**
(45) **Date of Patent: Dec. 7, 2021**

(54) **MULTI-DIE MEMORY DEVICE**

(71) Applicant: **Rambus Inc.**, San Jose, CA (US)

(72) Inventors: **Scott C. Best**, Palo Alto, CA (US); **Ming Li**, Fremont, CA (US)

(73) Assignee: **Rambus Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/135,112**

(22) Filed: **Dec. 28, 2020**

(65) **Prior Publication Data**

US 2021/0193215 A1 Jun. 24, 2021

Related U.S. Application Data

(63) Continuation of application No. 16/823,122, filed on Mar. 18, 2020, now Pat. No. 10,885,971, which is a (Continued)

(51) **Int. Cl.**
G11C 5/02 (2006.01)
G11C 11/4093 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G11C 11/4093*** (2013.01); ***G11C 5/02*** (2013.01); ***G11C 5/025*** (2013.01); ***G11C 5/04*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC ... G11C 11/4093; G11C 11/02; G11C 11/025; G11C 11/04
(Continued)

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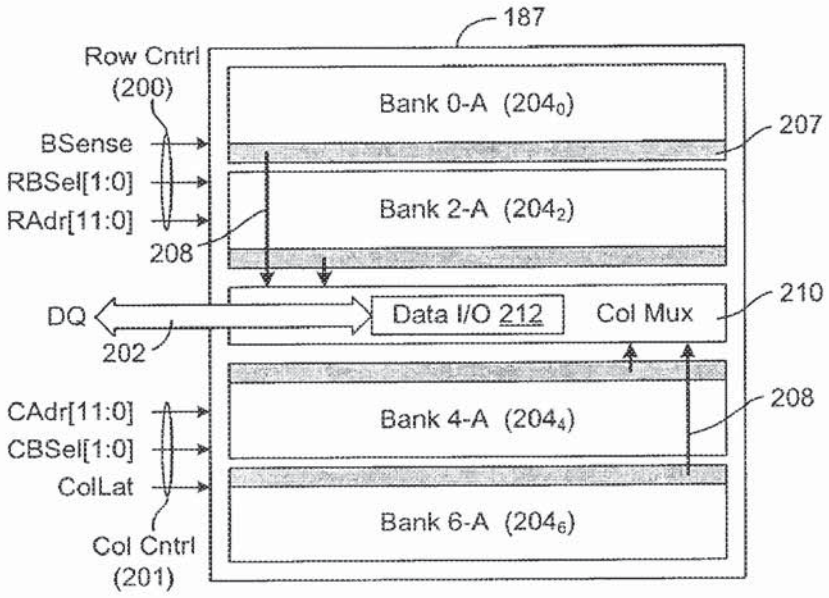
Primary Examiner — Vu A Le
(74) *Attorney, Agent, or Firm* — Lance Kreisman; Peninsula Patent Group

(57) **ABSTRACT**

A memory is disclosed that includes a logic die having first and second memory interface circuits. A first memory die is stacked with the logic die, and includes first and second memory arrays. The first memory array couples to the first memory interface circuit. The second memory array couples to the second interface circuit. A second memory die is stacked with the logic die and the first memory die. The second memory die includes third and fourth memory arrays. The third memory array couples to the first memory interface circuit. The fourth memory array couples to the second memory interface circuit. Accesses to the first and third memory arrays are carried out independently from accesses to the second and fourth memory arrays.

20 Claims, 12 Drawing Sheets



Related U.S. Application Data

continuation of application No. 16/211,966, filed on Dec. 6, 2018, now Pat. No. 10,607,691, which is a continuation of application No. 15/809,925, filed on Nov. 10, 2017, now Pat. No. 10,157,660, which is a continuation of application No. 15/098,269, filed on Apr. 13, 2016, now Pat. No. 9,818,470, which is a continuation of application No. 14/797,057, filed on Jul. 10, 2015, now Pat. No. 9,324,411, which is a continuation of application No. 14/278,655, filed on May 15, 2014, now Pat. No. 9,082,463, which is a continuation of application No. 13/562,242, filed on Jul. 30, 2012, now Pat. No. 8,737,106, which is a continuation of application No. 12/519,353, filed as application No. PCT/US2007/087359 on Dec. 13, 2007, now Pat. No. 8,233,303.

(60) Provisional application No. 60/870,065, filed on Dec. 14, 2006.

(51) **Int. Cl.**

G11C 11/4096	(2006.01)
G11C 5/04	(2006.01)
H01L 25/065	(2006.01)
H01L 25/10	(2006.01)
H01L 25/18	(2006.01)
H01L 23/48	(2006.01)
G11C 11/406	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 11/406*** (2013.01); ***G11C 11/4096*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 25/0652*** (2013.01); ***H01L 25/0657*** (2013.01); ***H01L 25/105*** (2013.01); ***H01L 25/18*** (2013.01); *H01L 24/73* (2013.01); *H01L 2224/0401* (2013.01); *H01L 2224/16225* (2013.01); *H01L 2224/32145* (2013.01); *H01L 2224/32225* (2013.01); *H01L 2224/48091* (2013.01); *H01L 2224/48225* (2013.01); *H01L 2224/48227* (2013.01); *H01L 2224/73265* (2013.01); *H01L 2225/0651* (2013.01); *H01L 2225/0652* (2013.01); *H01L 2225/06541* (2013.01); *H01L 2225/06558* (2013.01); *H01L 2225/06562* (2013.01); *H01L 2225/1023* (2013.01); *H01L 2225/1058* (2013.01); *H01L 2924/00011* (2013.01); *H01L 2924/00014* (2013.01); *H01L 2924/01019* (2013.01); *H01L 2924/01055* (2013.01); *H01L 2924/14* (2013.01); *H01L 2924/15311* (2013.01); *H01L 2924/15321* (2013.01); *H01L 2924/15331* (2013.01); *H01L 2924/3011* (2013.01)

(58) **Field of Classification Search**

USPC 365/51

See application file for complete search history.

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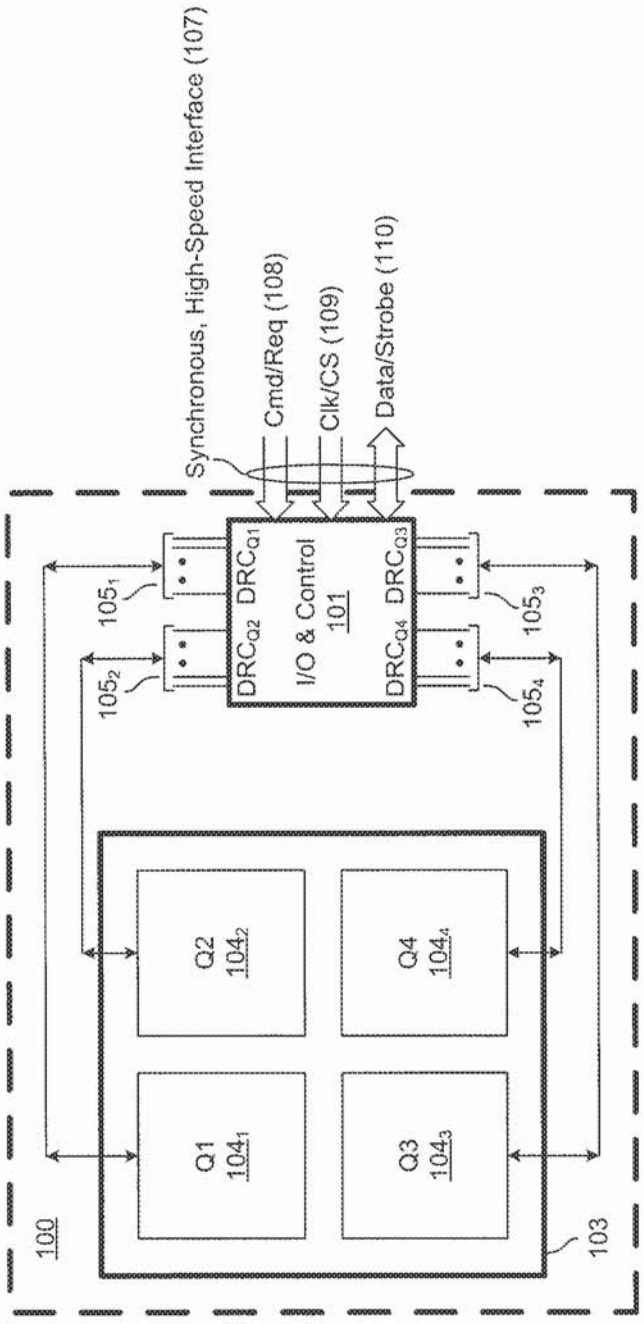
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Clk/CS (109)
Data/Strobe (110)
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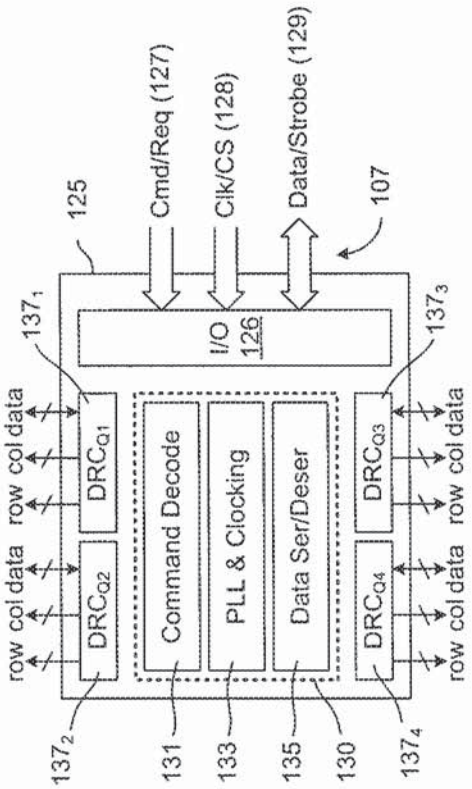
DRCQ2
DRCQ3
DRCQ4
1051
1052
1053
1054
Q1 1041
Q2 1042
Q3 1043
Q4 1044
100
103

FIG. 1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Data/Strobe (129)
107
I/O 126
1371
1373
row col data
DRCQ1
DRCQ2
DRCQ3
DRCQ4
Command Decode
PLL & Clocking
Data Ser/Deser
1372
131
133
135
130
1374

FIG. 2

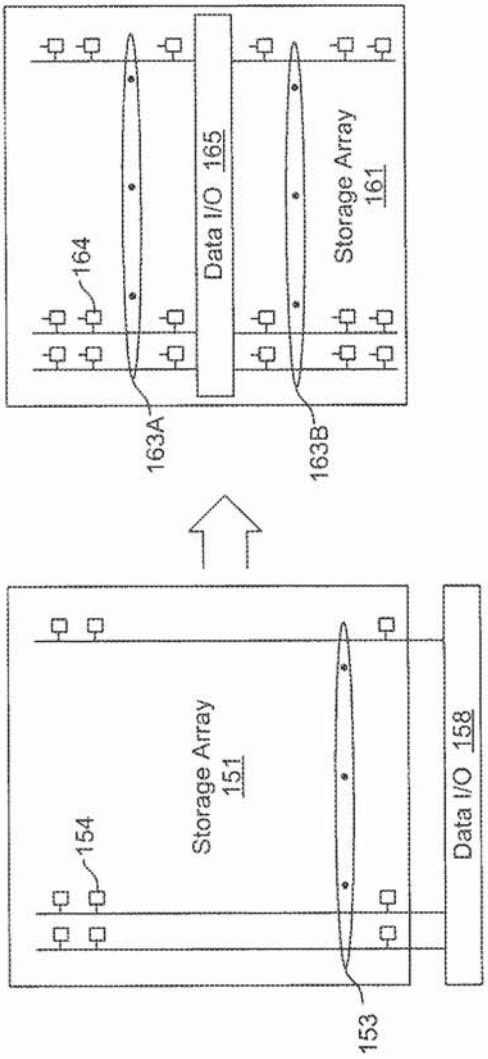


FIG. 4

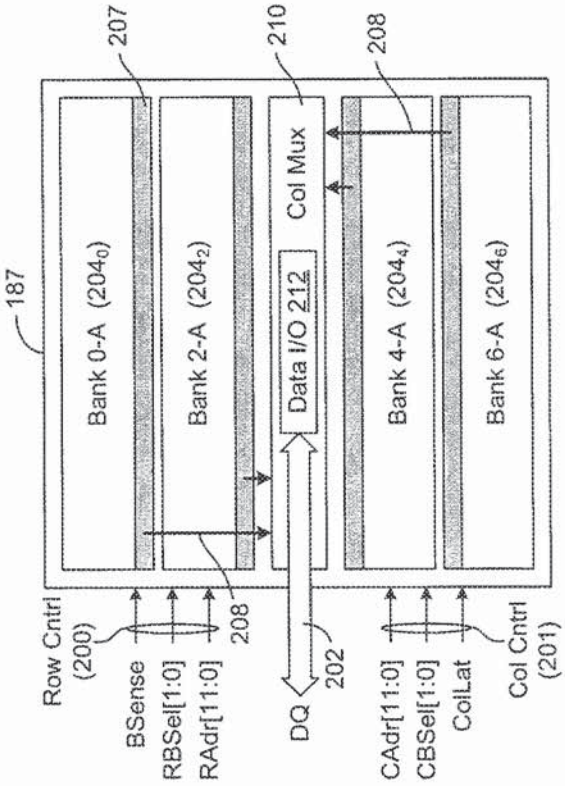


FIG. 5B

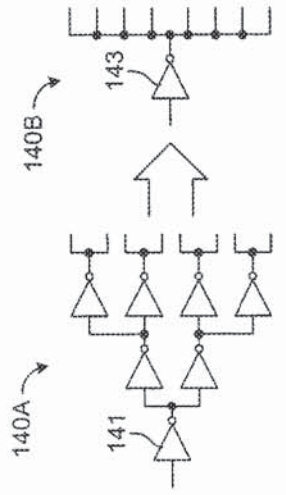


FIG. 3

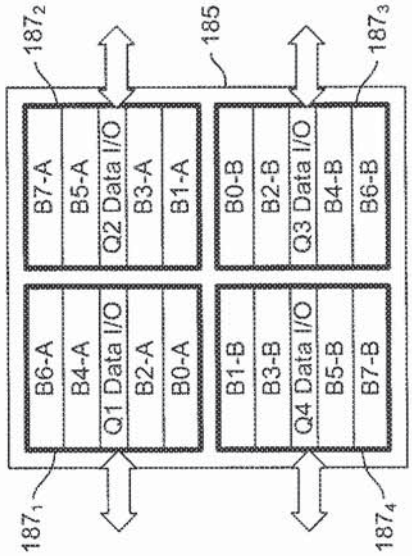


FIG. 5A

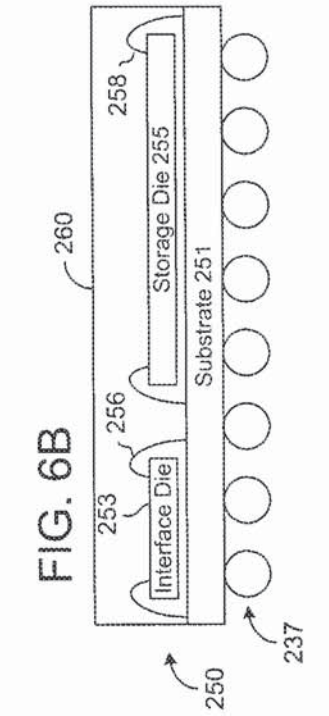


FIG. 6B

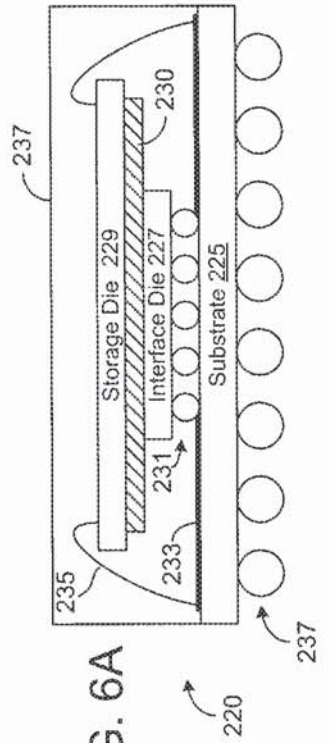
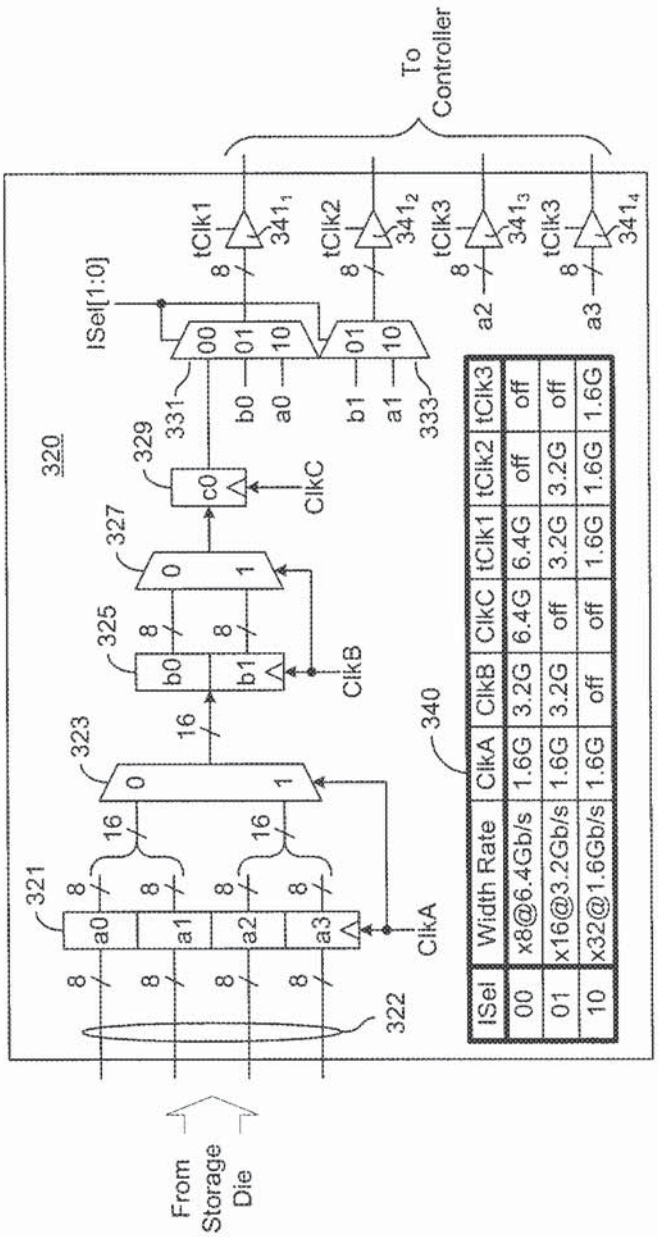


FIG. 6A



ISel	Width Rate	ClkA	ClkB	ClkC	tClk1	tClk2	tClk3
00	x8@6.4Gb/s	1.6G	3.2G	6.4G	6.4G	off	off
01	x16@3.2Gb/s	1.6G	3.2G	off	3.2G	3.2G	off
10	x32@1.6Gb/s	1.6G	off	off	1.6G	1.6G	1.6G

FIG. 7B

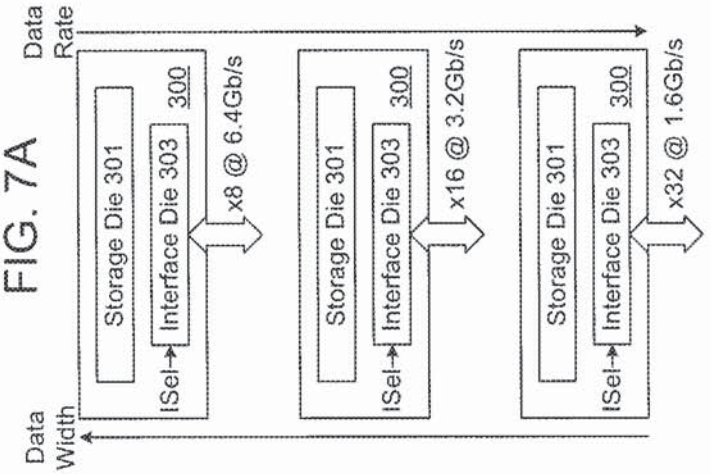


FIG. 7A

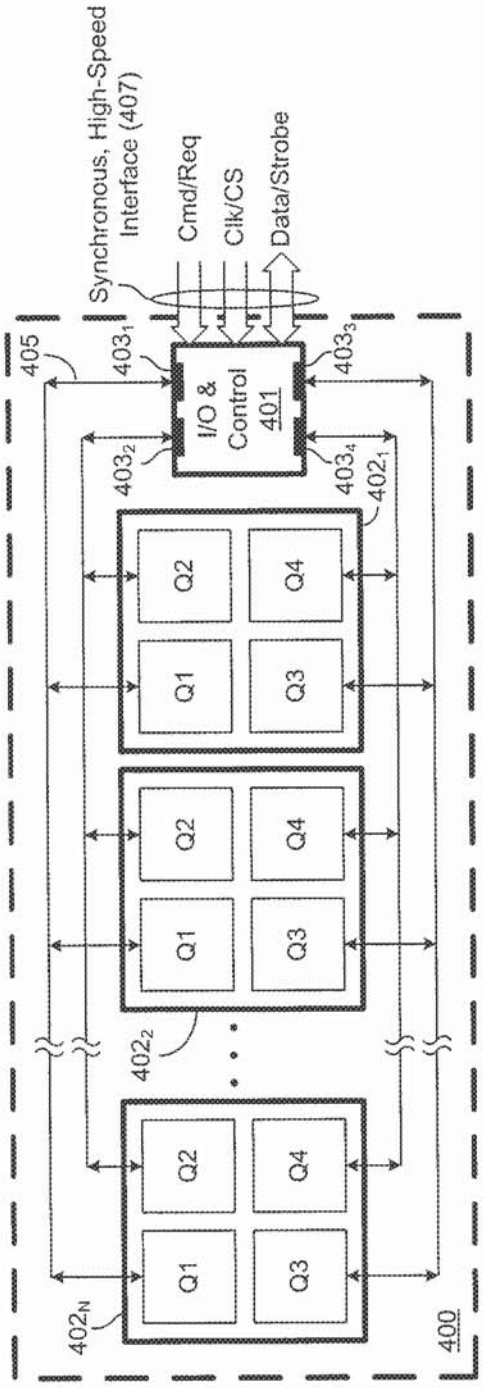
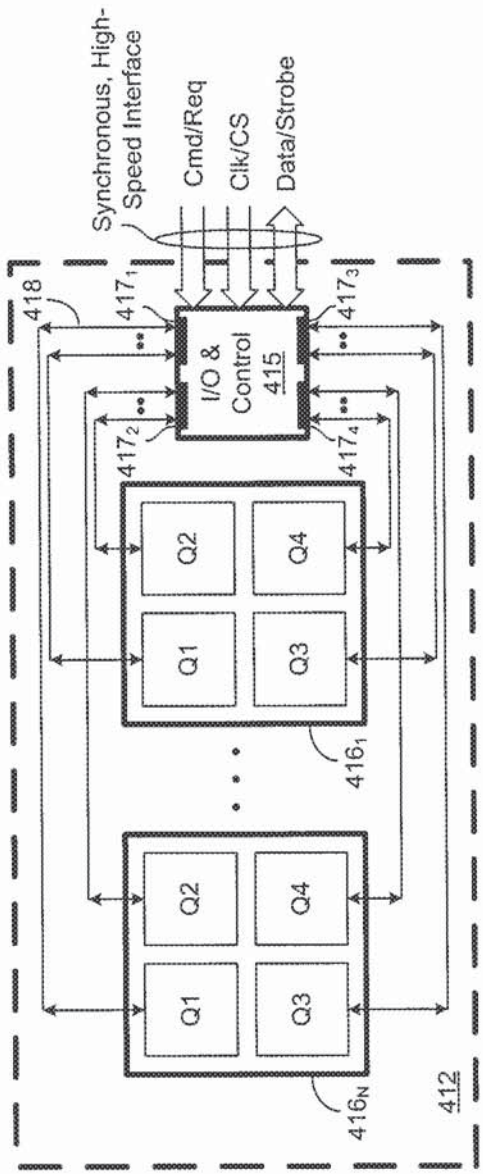

Synchronous, High-Speed Interface (407)
Cmd/Req
Clk/CS
Data/Strobe
405
403_1
403_2
403_3
403_4
I/O & Control 401
402_1
402_2
402_N
Q1
Q2
Q3
Q4
400

FIG. 8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Q2
Q3
Q4
412

FIG. 9

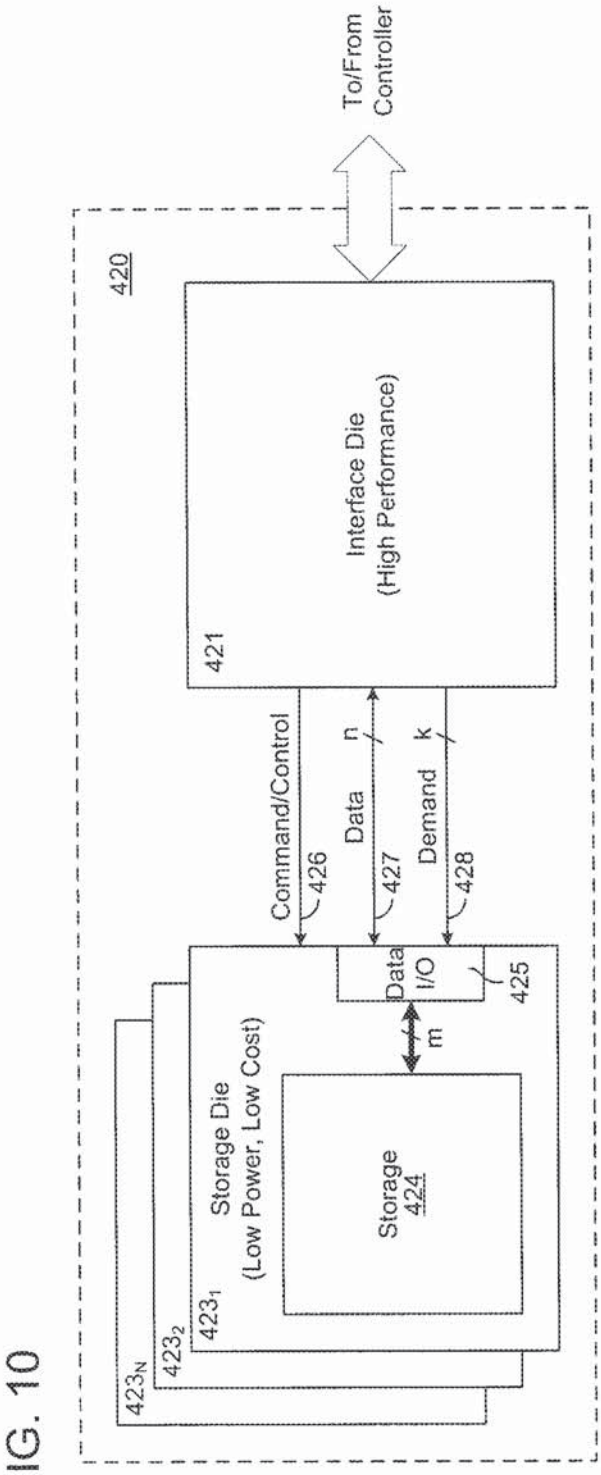
To/From Controller
420
Interface Die (High Performance)
421
Command/Control
426
Data
n
427
Demand
k
428
Data I/O
425
m
Storage Die (Low Power, Low Cost)
Storage 424
423_1
423_2
423_N

FIG. 10

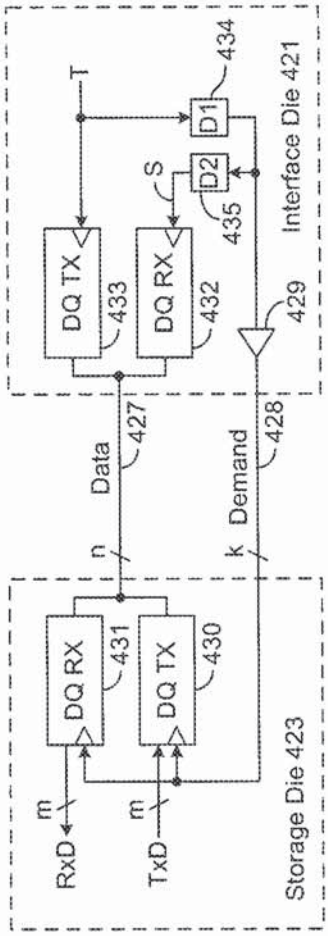
T
434
D1
S
D2
435
DQ TX
433
DQ RX
432
429
Interface Die 421
Data
427
n
Demand
428
k
DQ RX
431
DQ TX
430
m
RxD
m
TxD
Storage Die 423

FIG. 11

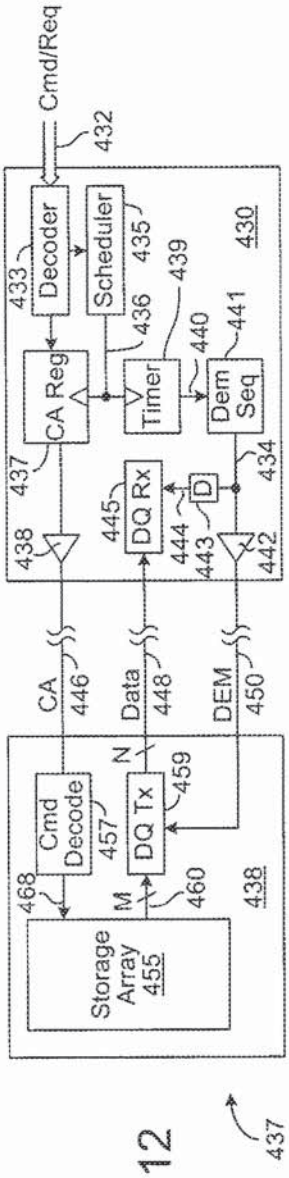

FIG. 12

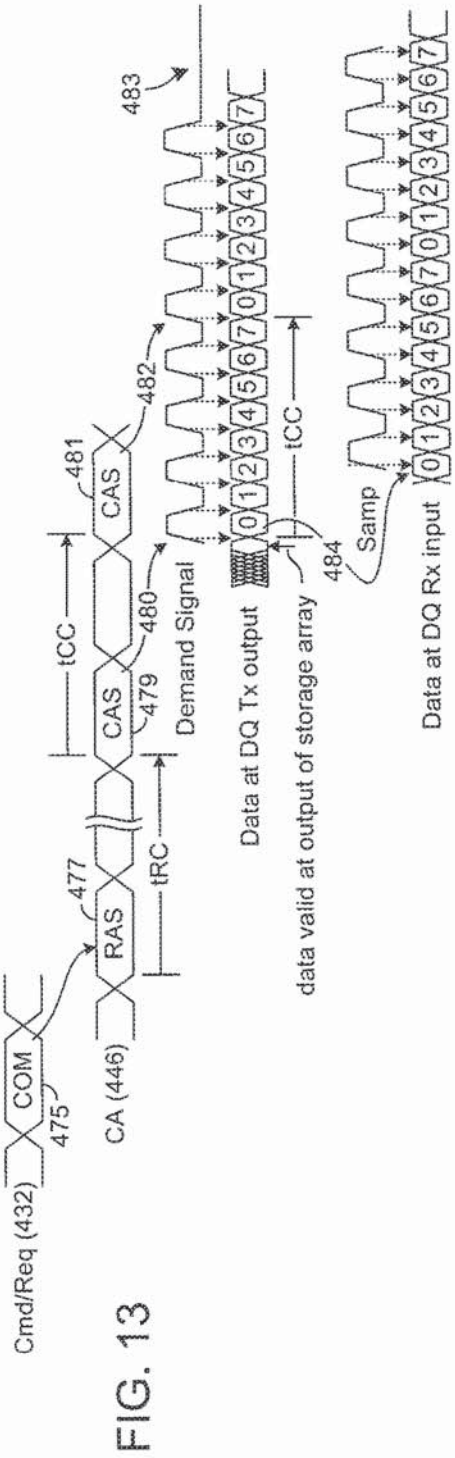

FIG. 13

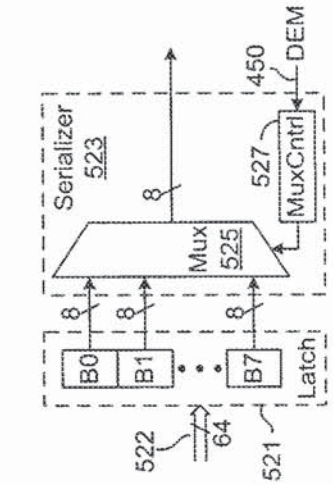

FIG. 15

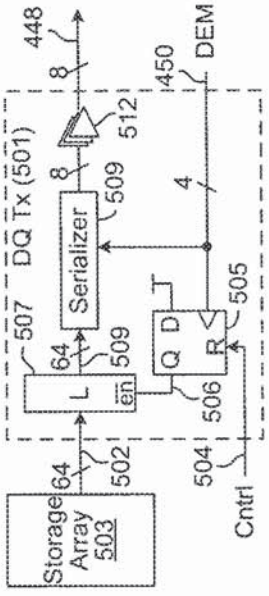

FIG. 14

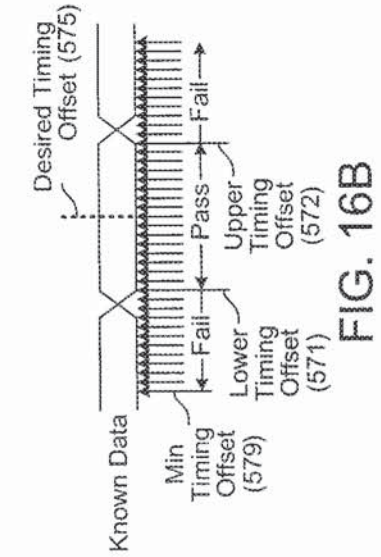

FIG. 16B

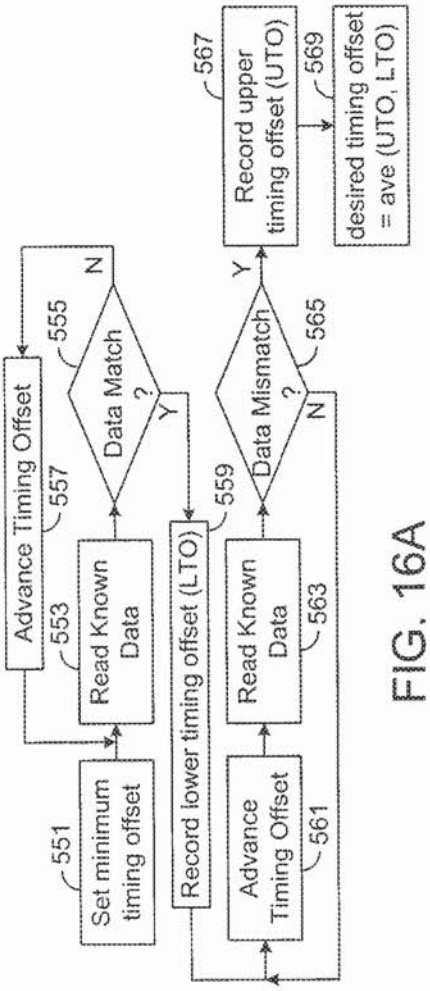

FIG. 16A

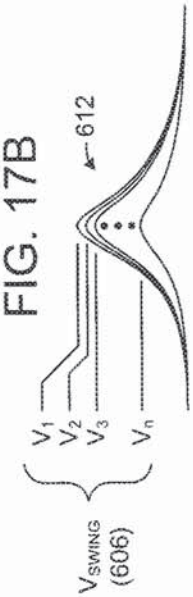

FIG. 17B

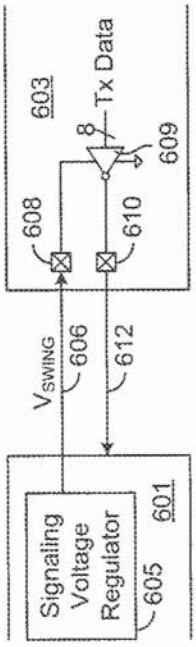

FIG. 17A

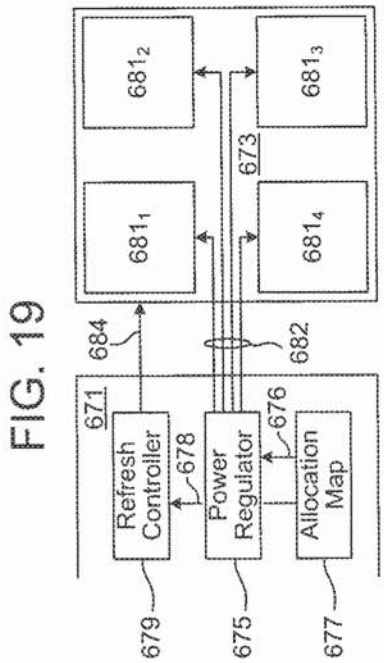

FIG. 19

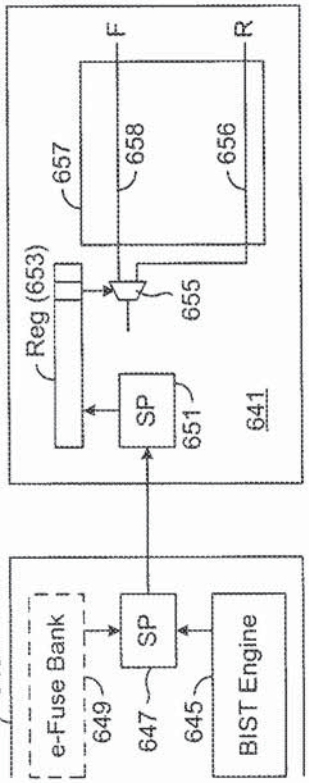

FIG. 18

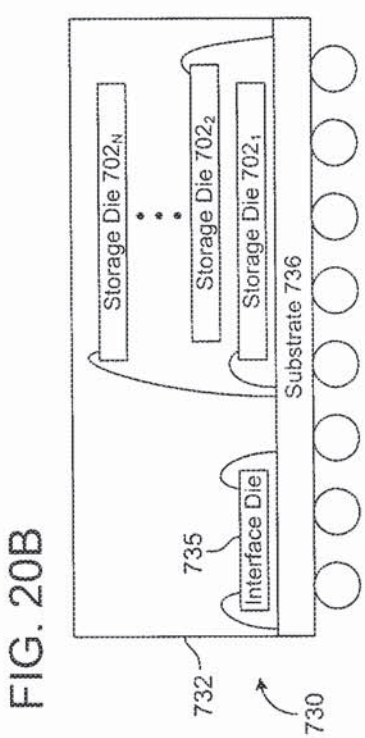

FIG. 20B

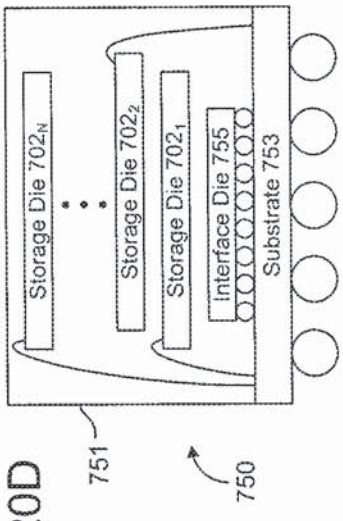

FIG. 20D

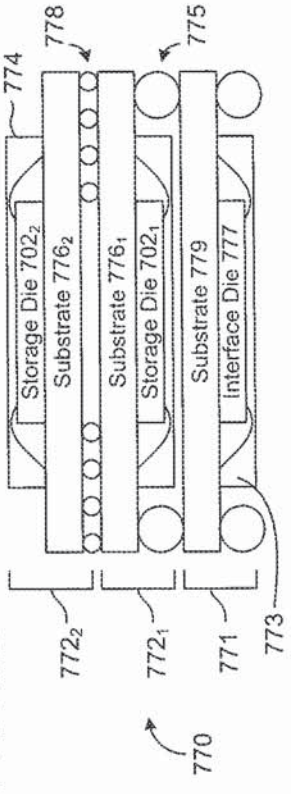

FIG. 20F

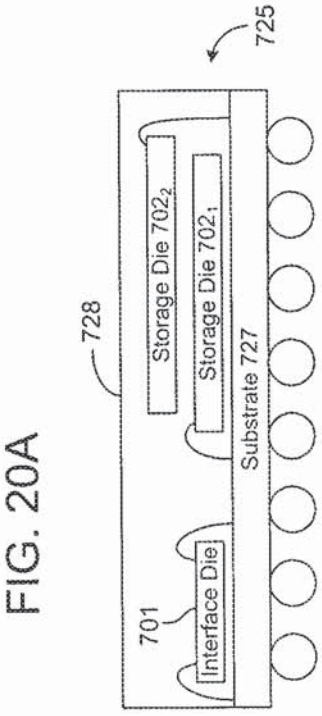

FIG. 20A

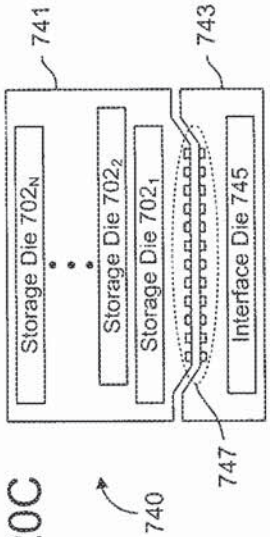

FIG. 20C

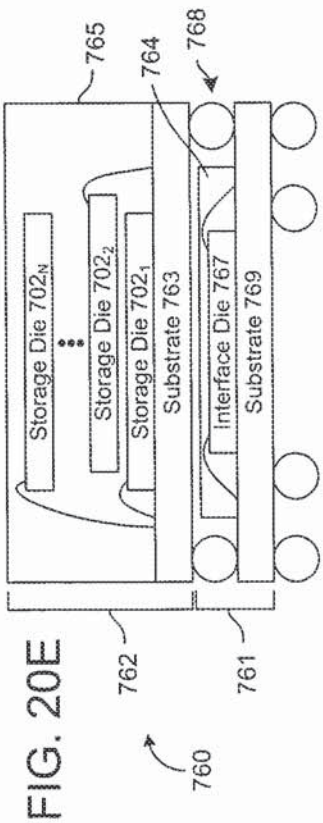

FIG. 20E

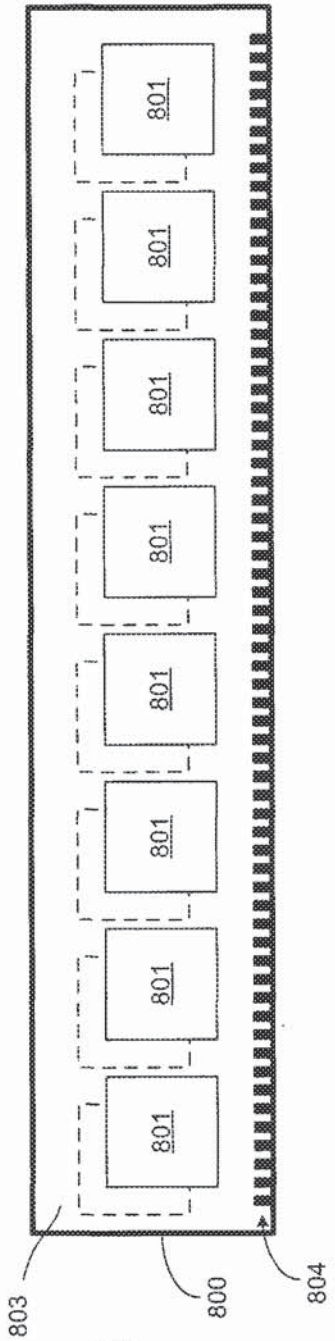
801
801
801
801
801
801
801
801
803
800
804

FIG. 21

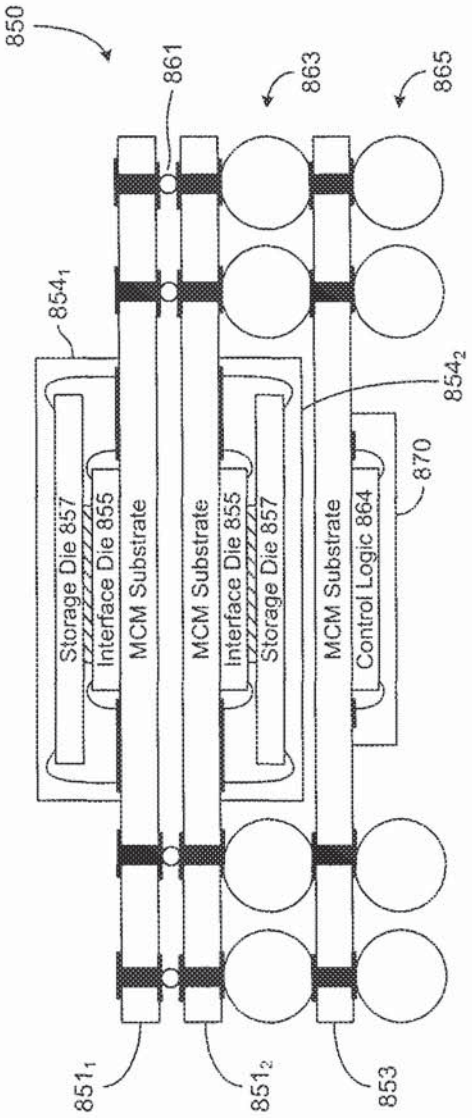
850
861
863
865
854_1
854_2
Storage Die 857
Interface Die 855
MCM Substrate
MCM Substrate
Interface Die 855
Storage Die 857
MCM Substrate
Control Logic 864
870
851_1
851_2
853

FIG. 22

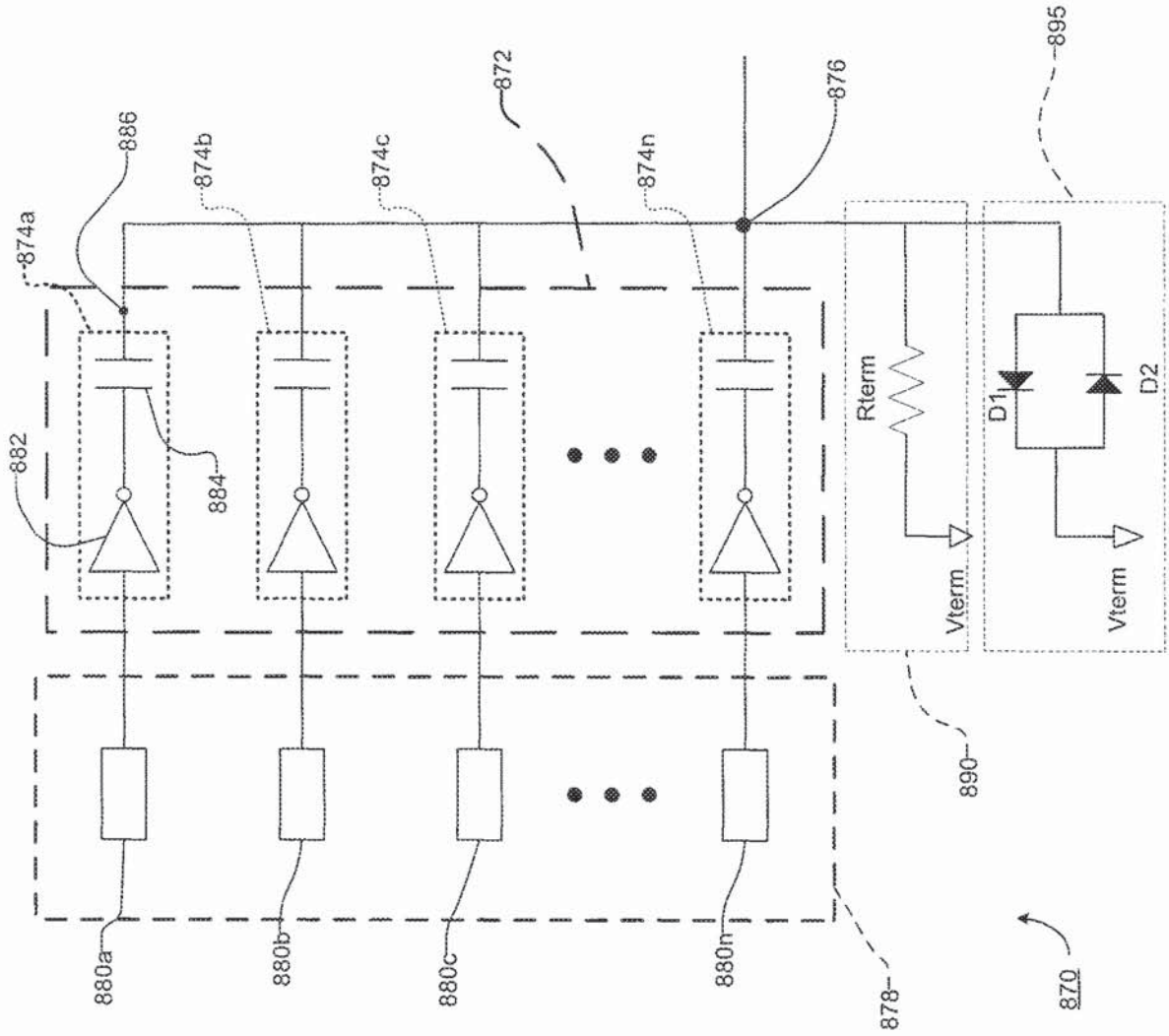
895
872
876
886
874b
874c
874n
874a
Rterm
D1
D2
882
884
Vterm
Vterm
890
880a
880b
880c
880n
878
870

FIG. 23

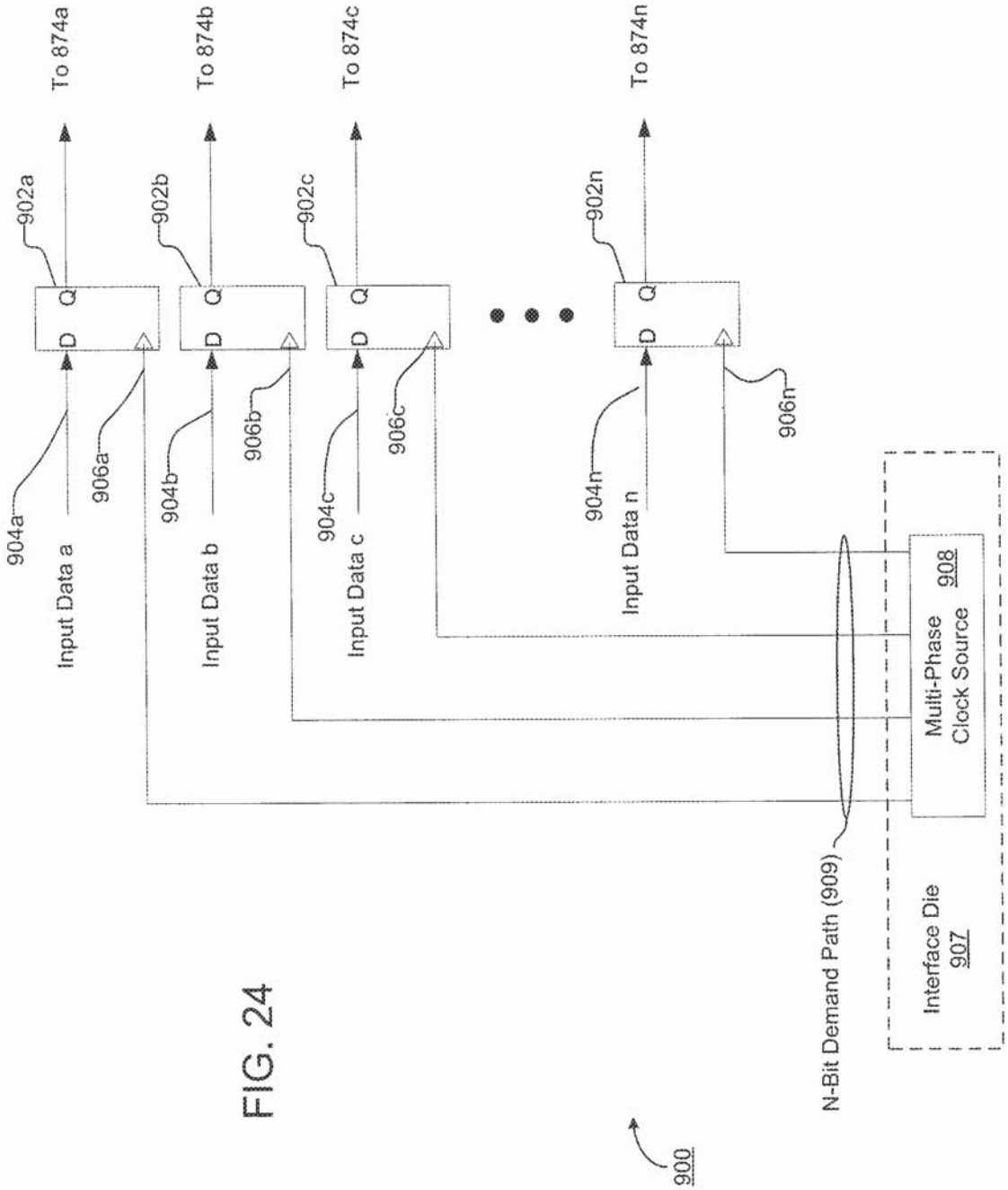
To 874a
To 874b
To 874c
To 874n
902a
902b
902c
902n
Q
D
904a
904b
904c
904n
906a
906b
906c
906n
Input Data a
Input Data b
Input Data c
Input Data n
Multi-Phase Clock Source 908
Interface Die 907
N-Bit Demand Path (909)
900

FIG. 24

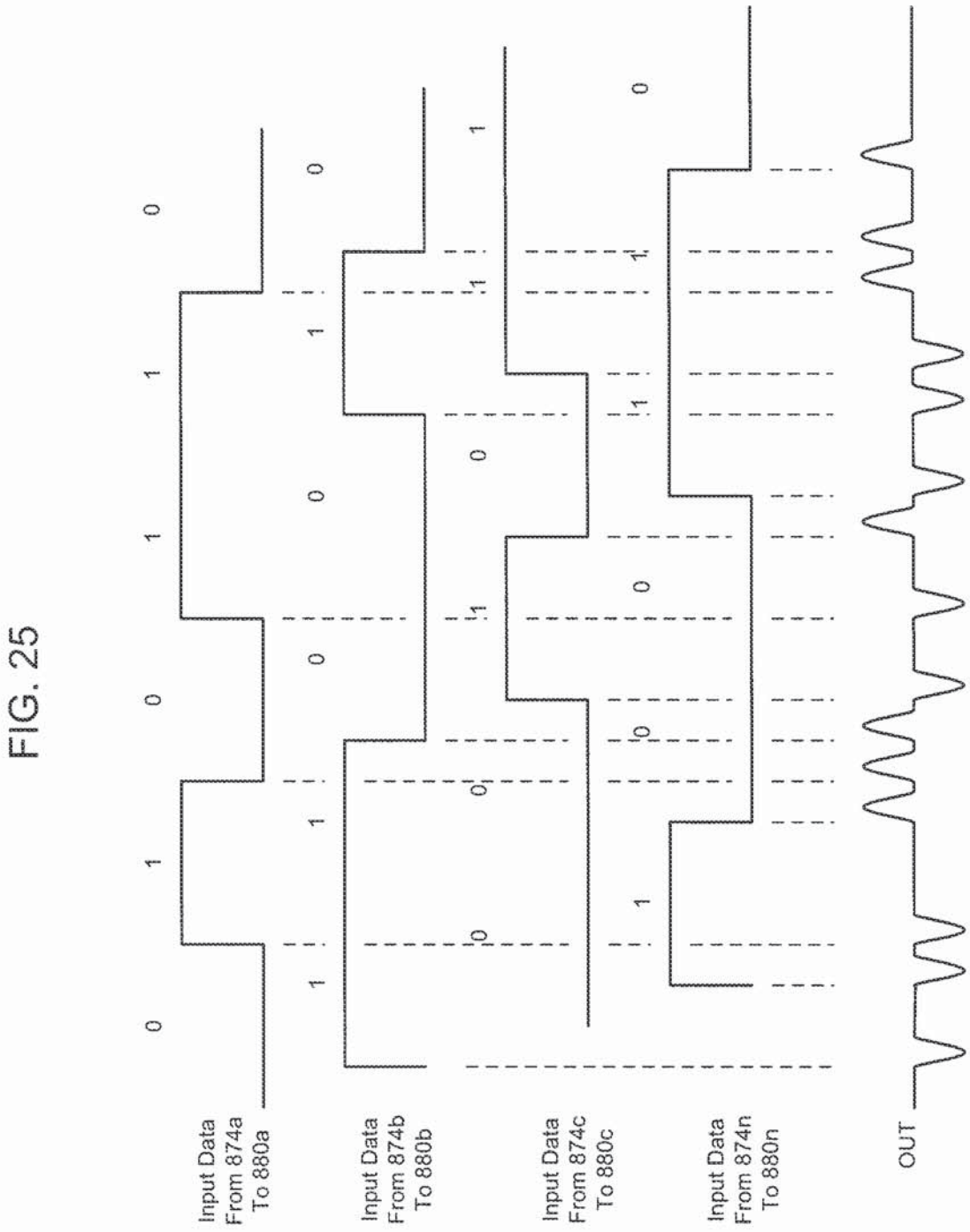
Input Data From 874a To 880a
Input Data From 874b To 880b
Input Data From 874c To 880c
Input Data From 874n To 880n
OUT

FIG. 25

MULTI-DIE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. Ser. No. 16/823,122, filed Mar. 18, 2020, entitled MULTI-DIE MEMORY DEVICE, which is a Continuation of U.S. Ser. No. 16/211,966, filed Dec. 6, 2018, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 10,607,691, which is a Continuation of U.S. Ser. No. 15/809,925, filed Nov. 10, 2017, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 10,157,660, which is a Continuation of U.S. Ser. No. 15/098,269, filed Apr. 13, 2016, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 9,818,470, which is a Continuation of U.S. Ser. No. 14/797,057, filed Jul. 10, 2015, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 9,324,411, which is a Continuation of U.S. Ser. No. 14/278,655, filed May 15, 2014, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 9,082,463, which is a Continuation of U.S. Ser. No. 13/562,242, filed Jul. 30, 2012, entitled MULTI-DIE MEMORY DEVICE, now U.S. Pat. No. 8,737,106, which is a Continuation of U.S. Ser. No. 12/519,353, filed Jun. 15, 2009, entitled MULTI-DIE MEMORY DEVICE, issuing as U.S. Pat. No. 8,233,303 on Jul. 31, 2012, which claims priority under 35 U.S.C. § 365 to International Application No. PCT/US2007/087359, filed Dec. 13, 2007, published as WO 2008/076790 A2 on Jun. 26, 2008, which claims priority under 35 U.S. C. § 119(e) to U.S. Provisional Application No. 60/870,065, filed Dec. 14, 2006, entitled MULTI-DIE MEMORY DEVICE, all of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

The present invention relates to data storage technology.

BACKGROUND

Power consumption in dynamic random access memory (DRAM) devices has historically scaled in proportion to the product of signaling bandwidth and storage capacity. As more applications demand higher performance and higher capacity, DRAM power consumption is projected to increase dramatically, presenting substantial cooling challenges for system designers and making advances in signaling rate and capacity increasingly difficult.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. **1** illustrates an embodiment of an integrated circuit package having synchronous, high-speed interface and core storage functions split between an interface die and a storage die, respectively;

FIG. **2** illustrates an embodiment of an interface die that may be used to implement the interface die of FIG. **1**;

FIG. **3** illustrates a portion of a inverter-based clock distribution circuit implemented in a conventional DRAM process and a counterpart inverter-based clock distribution circuit implemented in a high-speed logic process;

FIG. **4** illustrates a comparison between a conventional arrangement of a storage array coupled to a centralized I/O and an arrangement that may be used within the storage die of FIG. **1**;

FIG. **5**A illustrates an exemplary arrangement of storage arrays within a storage die and FIG. **5**B illustrates a more detailed embodiment of a representative storage array within the arrangement of FIG. **5**A;

FIGS. **6**A and **6**B illustrate embodiments of multi-component packages having separate storage and interface dice;

FIG. **7**A illustrates an embodiment of a multi-die memory device having an interface die that may be configured at run-time or production time to establish a selected interface data width and data rate;

FIG. **7**B illustrates an exemplary serializing circuit that may be provided within an interface die to support configurable serialization of read data returned from a storage die within a multi-die memory device;

FIG. **8** illustrates an alternative embodiment of a multi-die memory device having multiple storage dice coupled to a shared interface die;

FIG. **9** illustrates an alternative embodiment of a multi-die memory device in which an interface die includes a dedicated set of data interfaces for each storage die;

FIG. **10** illustrates an embodiment of a multi-die memory device in which an interface die outputs a demand signal to a selected one of multiple storage dice to enable read-data output;

FIG. **11** illustrates an embodiment of a timing arrangement for bi-directional data transmission between the storage die and interface die of FIG. **10**;

FIG. **12** illustrates a more detailed embodiment of a multi-die memory device in which a demand signal is used to effect time-multiplexed read data transfer between an interface die and a storage die;

FIG. **13** illustrates an exemplary memory-read command sequence and corresponding read data transfer sequence within the multi-die memory device of FIG. **12**;

FIG. **14** illustrates an embodiment of a data transmit circuit that may be used to implement data transmitter of FIG. **12**;

FIG. **15** illustrates embodiments of a serializer and latch that may be used to implement the serializer and latch of FIG. **14**;

FIGS. **16**A and **16**B illustrate an exemplary timing calibration operation that may be carried out by the interface die of FIG. **12** to determine an appropriate time delay between assertion of the demand signal and assertion of the corresponding read data sampling signal;

FIG. **17**A illustrates a multi-die memory device having an interface die that provides one or more supply voltages to output drivers within a counterpart storage die to control the amplitude of output signals generated by the storage die;

FIG. **17**B illustrates amplitudes of exemplary output signals generated by the storage die of FIG. **17**A in response to different supply voltages from the counterpart interface die;

FIG. **18** illustrates a multi-die memory device having an interface die with built-in self-test circuitry and redundancy control circuitry;

FIG. **19** illustrates an embodiment of a multi-die memory device in which an interface die includes a power regulator to selectively power each of multiple storage arrays \ within a storage die;

FIG. **20**A illustrates an exemplary packaging arrangement that may be used to encapsulate a pair of storage dice within a multi-die memory device;

FIG. **20**B illustrates an exemplary packaging arrangement that may be used to encapsulate a generalized number of storage dice within a multi-die memory device;

FIG. **20**C illustrates another packaging arrangement in which an interface die and storage die are packaged separately in packages that mate to one another to form a multi-package module;

FIG. **20**D illustrates another packaging embodiment in which an interface die is mounted in a flip-chip orientation to a module substrate;

FIG. **20**E illustrates a package-on-package embodiment having a storage package stacked on an interface package;

FIG. **20**F illustrates another package-on-package embodiment having multiple storage packages stacked on an interface package;

FIG. **21** illustrates an embodiment of a memory module having rows of multi-die memory devices disposed on front and rear faces;

FIG. **22** illustrates a memory subsystem that includes a memory controller and a pair of multi-die memory devices disposed in a package-on-package arrangement;

FIG. **23** illustrates a high-level block diagram of a pulsed signaling multiplexer that may be used to perform serializing operations and other functions within a storage die and/or interface die within a multi-component package or other multi-chip package;

FIG. **24** illustrates a timing circuit that may be used in conjunction with the multiplexer of FIG. **23**; and

FIG. **25** illustrates a timing diagram for the multiplexer of FIG. **23**.

DETAILED DESCRIPTION

A memory device having storage and control functions split between separate integrated circuit dice within a multi-die integrated circuit package is disclosed in various embodiments. In particular, recognizing that compromises inherent in conventional DRAM fabrication processes yield relatively inefficient high-speed logic circuitry, reduced power may be achieved by relegating the high-speed circuitry that forms the control and signaling interface of a conventional memory device to a separate interface die that is fabricated using a process that yields power-efficient high-speed circuitry. With most or all of the high-speed circuitry removed, the core storage circuitry that remains on the storage die may be fabricated in a process that is more appropriate to balancing cell retention time and storage density, potentially saving additional power. Also, by disposing the interface die and the storage die in close proximity to one another within a common integrated circuit (IC) package (e.g., a multi-component package (MCP) such as a stacked package die, also known as a multi-die package (MDP), multi-chip module (MCM), system-in-package (SIP), etc.), a substantially larger number of die-to-die interconnections may be achieved than if each of the dice is enclosed within separate IC packages. In particular, in one embodiment, the larger number of die-to-die interconnects possible within a multi-die package are applied to establish a dedicated set of control and data signal paths between the interface die and each of multiple storage arrays within the storage die. In one embodiment, the intra-package data signal interconnects are disposed at a central region within each of the storage arrays of the storage die thus enabling substantially shorter bit lines to be used than in arrangements having bit lines that traverse the entire storage array, thereby increasing data retrieval speed and/or significantly reducing access power at nominal speeds.

In one embodiment, the interface die and storage die are disposed in a stack (i.e., one on top of another) on top of a multi-die package substrate. The top die in the stack, which may be the interface die or the storage die, may be wire-bonded to conductive traces or other conductive structures in the package substrate to establish connection to the bottom die. The bottom die may also be wire bonded to the conductive structures within the package substrate or may be coupled to the conductive structures via flip-chip arrangement or any other interconnection arrangement. In another embodiment, the interface die and storage die may be mounted side-by-side on the package substrate, and may be directly wire bonded to one another and/or flip-chip-interconnected or wire-bond-interconnected through conductive structures in the package substrate. There are many other embodiments in which the interface die is interconnected to the storage die using a variety of "3D packaging" technologies including, but not limited to, thru-silicon vias, flex-tape, die-in-substrate encapsulation, direct wafer bonding, proximity interconnect, and so forth. In any of these variants, the MCP may include an encapsulating structure or other housing disposed over the interface die and storage die to form an integrated-circuit (IC) package. Further, the separate interface and storage dice may cooperate to mimic the functional operation of conventional memory devices and the multi-die memory package may be form-factor and contact-compatible with such memory devices. Accordingly, the multi-die memory device may be disposed in place of conventional memory devices on memory modules, motherboards, or in any other application where conventional memory devices may be applied. Further, additional storage dice may be included within the multi-die memory device, each coupled to the interface die but omitting full-time clocked input/output circuitry and thus multiplying storage capacity without substantially increasing static power consumption. These and other embodiments are described in further detail below.

FIG. **1** illustrates an embodiment of an IC package **100** having synchronous, high-speed interface and core storage functions split between an interface die **101** and a storage die **103**, respectively. The interface die **101**, also called an I/O and control die, includes a high-speed interface **107** and multiple internal memory array interfaces $\mathbf{105}_1$-$\mathbf{105}_4$. In the embodiment of FIG. **1**, the high-speed interface **107** is a synchronous interface that receives timing signals and memory access commands from an external memory controller (not shown), and that receives write data in conjunction with memory write commands and outputs read data in response to memory read commands. In a particular embodiment, the high-speed interface **107** may be designed to mimic the interface of a conventional memory device and thus may receive commands (or requests) via a command path **108** (Cmd/Req) synchronously with respect to a clock signal received via a clock/chip-select path **109** (Clk/CS), and may receive data via a data path **110** (Data/Strobe) in response to transitions of corresponding strobe signals (i.e., timing references) conveyed source synchronously on strobe lines within the data path **110**. The high-speed interface **107** may additionally include timing circuitry such as a phase-locked loop (PLL) or delay-locked loop (DLL) circuitry to generate an internal clock signal based on a reference clock signal received via the clock path **109**. In one embodiment, for example, the internal clock signal is used to sample command signals conveyed via the command path **108**, and to generate strobe signals that are output via data path **110** in conjunction with read data, thereby providing a source-synchronous timing reference for establishing a read-data sampling time within the external memory controller. The timing circuitry within the high-speed interface **107** may additionally include phase adjustment circuitry to enable

desired phase offsets between the internal clock signal and reference clock signal and/or between data signal sampling times and transitions in corresponding incoming data strobe signals.

In the embodiment of FIG. **1**, each of the memory array interfaces **105**$_1$-**105**$_4$ (DRC$_{Q1}$-DRC$_{Q4}$) is coupled to a respective storage array **104**$_1$-**104**$_4$ within the storage die **103**, and includes a relatively slow and wide data path (i.e., relative to the high-speed interface **107**) that, in one embodiment, matches the column access width of the storage array, as well as an asynchronous command path for conveying row and column control signals to the storage array. That is, the command transfer from interface die **101** to storage die **103** is clockless (or un-clocked) in that no periodic clock signal is conveyed along with the row and column control signals, though one or more non-periodic strobe signals such as row-address-strobe (RAS) and column-address-strobe signals (CAS) may be issued to initiate address latching and corresponding memory access operations within the storage die. By minimizing the use of free-running or continuous clocking circuitry on the storage-die, and instead having the interface die provide a timing reference signal only when needed (e.g., during signal transmission between the storage die and the interface die) substantial power savings can be realized. A clocked command path (and corresponding clocked interface in the storage die) may be used for command transfer in alternative embodiments. The data signal transfer between the interface die **101** and storage die **103** may be timed by a clock or strobe signal, or may be transmitted asynchronously. In the case of asynchronous data transmission, sampling time within the interface die **101** and/or storage die **103** may be established deterministically with respect to transmission or receipt of row/column control signals.

In the embodiment of FIG. **1**, the storage die **103** includes four independently accessible storage arrays **104**$_1$-**104**$_4$ (Q1-Q4 and also referred to herein as quadrants, though more or fewer arrays may be provided in alternative embodiments), each coupled to a respective one of the memory array interfaces **105**$_1$-**105**$_4$ within the interface die **101**. As discussed in further detail below, the separate signaling paths between the storage arrays **104** and the interface die **101** enable the storage arrays **104** to be designed with substantially shorter data bit lines than in conventional memory devices that have a single multiplexed I/O node.

FIG. **2** illustrates an embodiment of an interface die **125** that may be used to implement the interface die **101** of FIG. **1**. As shown, interface die **125** includes I/O circuitry **126** that forms at least a portion of the high-speed interface **107** described above, and includes a command interface **127** to receive commands (or requests) from an external control device, a clock/chip-select interface **128** to receive a reference clock signal, clock-enable signal, chip-select signal and other timing and/or control-related signals (e.g., serial I/O signals that may be used to configure the operation of the high-speed external interface prior to normal device operation), and a data I/O interface **129** to receive write data signals and corresponding strobe signals and mask signals, and to output read data and corresponding strobe signals. The input/output circuitry **126** is coupled to a core logic block **130** that includes command decode circuitry **131** (referred to herein as a command decoder), timing circuitry **133** and data serializing and deserializing circuitry **135**. In one embodiment, the timing circuitry **133** includes a PLL (a delay-locked loop or even open-loop delay line may alternatively be used) to receive the incoming reference clock signal and, when the clock-enable signal is asserted, to generate an internal clock signal (e.g., a frequency equivalent or frequency multiple of the reference clock) that is used to sample command signals arriving via the command path and to synchronize operations within the interface die **125**, including data serializing and deserializing operations. More specifically, the internal clock signal generated by the PLL may be supplied to a clock tree that distributes multiple delay-matched instances of the clock signal to various other circuit blocks within the interface die **125**, including the command decoder **131**, data serializing/deserializing circuitry **135** and I/O circuitry **126**.

The command decoder **131** buffers incoming memory access commands, determines which of the storage arrays **104** a given command is directed to, and converts the command into the row and/or column control signals needed to carry out the commanded operation. In one embodiment, for example, each incoming memory access command may be either a row command (e.g., an activation command or a precharge command) that includes bank and row addresses that uniquely identify a bank and storage row therein to be activated (or bank to be precharged), or a column command that includes bank and column addresses that uniquely identify the bank for which a row has been activated (i.e., contents of row transferred to set of sense amplifiers for the corresponding bank) and a column offset within the activated row. In the case of a row command, the command decoder converts the received bank and row address values into a set of row control signals and queues the row control signals to be output, in parallel, via an appropriate one of memory array interfaces **137**$_1$-**137**$_4$ (e.g., determined based on the bank address) a predetermined time (e.g., predetermined number of cycles of the internal clock signal) after the row command is received via the command interface **127**. Note that in an embodiment in which a storage bank is partitioned between two or more memory arrays of the storage die (e.g. elements **104**$_1$-**104**$_4$ of FIG. **1**), the row control signals may be queued for output to more than one of the storage arrays simultaneously (i.e., and thus, output via more than one of the memory array interfaces **137**$_1$-**137**$_4$). Similarly, in the case of a column command, the command decoder **131** converts the received bank and column address values into a set of column control signals and queues the column control signals to be output, in parallel, via one or more of the memory array interfaces **137**$_1$-**137**$_4$ a predetermined time after the column command is received via the command interface **127**.

In the case of a memory write operation, write data and corresponding data mask information is received via the data I/O interface **129** and deserialized to form a more parallel (i.e., wider) write data word that is output to the storage die via the data path coupled to an address-selected one of the storage arrays (i.e., via the data portion of one of memory array interfaces **137**$_1$-**137**$_4$). As an example, in one embodiment, write data is received synchronously in a sequence of 32-bit data transfers via the data I/O interface **129**, then deserialized to form a 128-bit write data word. The masking information (e.g., one mask bit per byte of write data) may be used to suppress output of selected bytes of the 128-bit write data word from the interface die **125**, thereby preventing the corresponding column locations within the storage die from being overwritten with write data. Alternatively, the masking information may be supplied to the storage die which itself may include circuitry to prevent data write in the indicated column locations. With respect to read and write data timing, in one embodiment, the data serializing and deserializing circuitry **135** may include read and write data queues to introduce a desired latency between receipt of a

write command via interface **127** and data transfer via the internal data path (i.e., write data transferred via the data portion of memory array interface **137**) or data I/O path **129** (read data).

As discussed above, splitting the high-speed interface circuitry and core storage circuitry between separate integrated circuit dice obviates process technology compromises, making it possible to fabricate high-speed interface circuitry in processes that yield faster, lower-gate-capacitance transistors and enabling the core storage circuitry to be implemented in processes that balance cell density and retention. The timing circuitry **133** and high-speed I/O circuitry **126**, in particular, tend to be come substantially more efficient when implemented in smaller-geometry processes. FIG. **3**, for example, illustrates a portion of a inverter-based clock distribution circuit **140**A implemented in a conventional DRAM process (e.g., an XXnm, dual gate-oxide DRAM process, where "XX" would be, for example, "90" for mainstream processes, 110 for trailing edge processes or 80 for leading edge processes) and a counterpart inverter-based clock distribution circuit **140**B implemented in a high-speed logic process (e.g., a YYnm, 1P6M CMOS process, where "XX" would be, for example, "90" for mainstream processes, "130" for trailing edge processes, and "65" for leading edge processes). In the conventional DRAM process, inverter fan-out is generally more limited due to the slower, higher gate capacitance transistors and thus typically requires multiple inverter stages to achieve a desired fan-out. In the particular example shown, fan-out is constrained to two loads per inverter **141** so that, to achieve a total fan-out of eight, seven inverters **141** are used. By contrast, because of the faster switching speed and lower gate capacitance achieved within the smaller-geometry process, each inverter **143** may drive as many as eight loads so that a single inverter **143** may be used to provide the same signal drive capability as the seven inverters **141** in FIG. **3**. Considering that all the inverters within the clock tree (and PLL and other interface circuitry) may be clocked near or above Gigahertz frequencies full-time during normal operation, the multi-fold reduction in clock tree and PLL components represents a substantial power savings within the multi-die memory module.

Another benefit of splitting the high-speed interface and storage core between separate integrated circuit dice is that data I/O connections may be provided separately to each storage array on the storage die, thus avoiding the need to route bit lines for each storage array to a centralized I/O circuit, as is the case when I/O circuitry is disposed centrally between multiple storage arrays in a memory IC. This approach is especially advantageous when combined with a 3D stacking technology (e.g., flip-chip bonding, thru-silicon via, die-in-substrate encapsulation, etc.), and/or a low-power, short-channel **10** interface technology (e.g., AC-coupled interconnect), that does not require the memory array contacts to be positioned at the edges of the memory die. FIG. **4**, for example, illustrates a comparison between a conventional arrangement of a storage array coupled to a centralized I/O circuit and an arrangement that may be used within the storage die **103** of FIG. **1**. As shown, the bit lines **153** within the conventional storage array **151** extend across virtually the entire length of the storage array to couple storage cells **154** to a mid-die data I/O circuit **158**. By contrast, in a storage array **161** that may be used to implement any of the storage arrays $\mathbf{104}_1$-$\mathbf{104}_4$ of FIG. **1**, a dedicated data I/O circuit **165** may be provided and therefore may be disposed centrally within the storage array **161**. By this arrangement, the bit lines of the storage array **161** may be split into two half-length bit line segments **163**A and **163**B that each extend from an outermost row of the storage array **161** to the centrally located (e.g., disposed at or near the midpoint between outermost rows) data I/O circuits, thereby roughly halving the capacitance of the storage array bit lines and thus reducing the time required to retrieve data from storage cells **164** in the outermost rows (the worst case and therefore limiting retrieval time) and also reducing power required to precharge the bit lines. Note that, while not shown in detail, the I/O circuit **165** may include sense amplifier circuitry and bank/column decode circuitry, or may be coupled to sense amplifier circuitry within individual storage banks of the storage array **161**.

FIG. **5**A illustrates an exemplary arrangement of storage arrays $\mathbf{187}_1$-$\mathbf{187}_4$ within a storage die **185** and FIG. **5**B illustrates a more detailed embodiment of a representative storage array **187**. In the embodiment shown, the storage die **185** includes four storage arrays $\mathbf{187}_1$-$\mathbf{187}_4$ (storage quadrants Q1-Q4), and eight storage banks, with each pair of cater-corner (i.e., diagonally opposed) storage arrays including the A and B segments, respectively, of a set of four storage banks. More specifically, odd-numbered storage quadrants Q1 and Q3 ($\mathbf{187}_1$ and $\mathbf{187}_3$) collectively include even numbered storage banks B**0**, B**2**, B**4** and B**6**, with bank segments B**0**-A, B**2**-A, B**4**-A and B**6**-A being disposed within quadrant Q1 ($\mathbf{187}_1$) and bank segments B**0**-B, B**2**-B, B**4**-B and B**6**-B being disposed within quadrant Q3 ($\mathbf{187}_3$). Odd numbered storage banks are similarly disposed in A and B segments within quadrants Q2 and Q4 ($\mathbf{187}_2$ and $\mathbf{187}_4$). As in all other storage die embodiments described herein, there may be more or fewer storage arrays per storage die, and more or fewer storage banks per storage array. Also, each storage bank may span more or fewer storage arrays than shown in FIGS. **5**A and **5**B.

Turning to FIG. **5**B, each of the storage arrays **187** includes a row decode circuit (not specifically shown) that responds to a bank-sense signal (B Sense) by selecting one of the four storage bank segments $\mathbf{204}_0$, $\mathbf{204}_2$, $\mathbf{204}_4$ or $\mathbf{204}_6$ (specified by a two-bit row-bank select value, RBSel[1:0]), and activating one of 4096 rows therein specified by a 12-bit row address value, RAdr[11:0]. Together, the bank sense, row-bank select, and row address value constitute, at least in part, exemplary row control signals **200** (other embodiments may use different signals that achieve the same or similar functionality). More or fewer banks **204** per storage array **187** and/or more or fewer rows per bank **204** may be provided in alternative embodiments, in which case RBSel and RAdr values may have more or fewer constituent bits. In the row activation operation, the contents of the activated row are transferred to a bank sense amplifier circuit **207** to enable write and read operations in response to column control signals **201**. More specifically, when a column-latch signal (ColLat) is asserted, the sense amplifier circuit **207** for the bank **204** specified by a column-bank select value, CBSel[1:0], is coupled via array bit lines **208** to a column decoder **210** (or column multiplexer) circuit disposed centrally within the storage array **187**, and a column address value, CAdr[11:0], is applied to couple a selected one of 4096 columns of array bit lines **208** to a data I/O circuit **212**, thereby enabling write data received via the data I/O circuit **212** to be driven onto the selected column of array bit lines **208** to overwrite data within the corresponding column of sense amplifiers within a bank-selected sense amplifier circuit **207**, or enabling read data to be output from the column of sense amplifiers to the data I/O circuit **212** and thus output to the interface die. Together, the column-latch signal, column-bank select value, and column address value

constitute, at least in part, exemplary column control signals **201** (other embodiments may use different signals that achieve the same or similar functionality).

Note that the individual storage arrays may be associated with different regions of a physical address space in a number of ways. For example, if there are sixteen storage arrays collectively within the set of storage dice, and the overall multi-die memory device is logically arranged as a four-bank device, then four storage arrays may be logically grouped together and associated with a single bank address. By this arrangement, a configurable number of storage banks may be established (e.g., through setting within a programmable register or other configuration circuit) and the total number of storage arrays dynamically allocated among each.

FIGS. **6**A and **6**B illustrate embodiments of multi-component packages **220** and **250** having separate storage and interface dice as described above. In the multi-component package **220** of FIG. **6**A, the interface die **227** and storage die **229** are disposed in a stack on a multi-component package (MCP) substrate **225**. In one embodiment, the substrate **225** is a non-conductive substrate having conductive vias therein to couple contacts of the interface die (the bottom die in the stack in this example) to ball grid array (BGA) contacts **237** for the multi-component package **220** (module contacts other than BGA may be used in alternative embodiments). The BGA contacts **237** may be soldered to counterpart landings on a daughterboard or motherboard (e.g., a memory module, blade, or motherboard of a data processing system, including various consumer electronics devices such as gaming consoles, mobile telephones, personal digital assistants (PDAs), cameras, audio and video rendering devices, etc.) and thus couple the multi-component package **220** to a larger electronics system. Within the multi-component package **220**, the interface die **227** may be wire-bonded to vias, traces or other conductive structures formed on or within the substrate **225** or may be coupled to the conductive structures via micro-BGA **231** or other flip-chip die-interconnect technology. The storage die **229** is disposed on top of the interface die **227** to form the die stack, and may be isolated from the interface die **227** by a dielectric spacer **230**. In the particular embodiment shown, the storage die **229** is wire-bonded (**235**) to conductive traces **233** disposed on the surface and/or sub-surface layers of the substrate **225**, the conductive traces **233** extending to the contacts of the interface die **227** to establish the intra-package interconnection between the interface die **227** and storage die **229**. Other 3D packaging approaches may be used to connect the interface die **227** with the substrate **225**, including, without limitation, thru-silicon vias, flex-tape, die-in-substrate encapsulation, direct wafer bonding, proximity interconnect, and so forth, with and without associated die-thinning techniques. A housing or cover **237** formed from plastic, ceramic or other non-conductive material may be disposed over the substrate, covering and protecting the die stack and interconnection structures.

FIG. **6**B illustrates an alternative embodiment of a multi-component package **250** in which an interface die **253** and storage die **255** are disposed side-by-side on a "System-in-Package" substrate **251**. As in the embodiment of FIG. **6**A, the substrate **251** may include conductive vias or other conductive structures to enable signal delivery via an external BGA **237** or other package interconnection technology, and may include conductive traces on the die-mount surface (or sub-surface layers) to which contacts on the storage die **255** and interface die **253** are wire bonded (**258**, **256**) to establish die-to-die interconnection. The interface die **253**, storage die **255** or both may alternatively be mounted in a flip-chip arrangement instead of being wire-bonded to the substrate conductors. Also, as in the embodiment of FIG. **6**A, a non-conductive housing or cover **260** may be disposed over the substrate **251** to protect the dice and interconnections structures.

FIG. **7**A illustrates an embodiment of a multi-die memory device having an interface die **303** that may be configured at run-time or production time to establish a selected interface data width, data rate, and electrical signaling levels. In the particular embodiment shown, the interface die may include a run-time programmable register, production-time programmable configuration circuit (e.g., fuse-programmable or anti-fuse-programmable circuitry) or input-signal configuration circuit (i.e., configuration determined by external inputs which may be strapped to high and low logic levels or delivered by another device) to enable selection between a 32-bit wide data interface at 1.6 Gigabit per second (Gb/s), a 16-bit wide data interface at 3.2 Gb/s or an 8-bit wide data interface at 6.4 Gb/s. Circuitry to support other data interface widths and/or data rates may be provided in alternative embodiments. However configured, an interface selection signal, ISel, may be provided to the interface die **303** to establish the interface characteristics, thus permitting the multi-die memory device to be applied in a variety of applications, for example, in place of various different conventional memory devices. Regardless of the selected interface characteristics, the interface die converts command and data signals as necessary to carry out data storage and retrieval operations within storage die **301**, thereby enabling application of the same storage die **301** in a broad variety of applications and thus providing the potential for volume production savings. Note also that a single storage die design with multiple, independently accessible storage arrays can be combined and interfaced with many different interface die designs, each with the same type of "internal memory interface," but different types of "external memory interface" each specific to a particular DRAM memory type with different bank counts and/or burst lengths (e.g., one that interfaces to standard DDR3 memory interfaces, another that interfaces to standard GDDR4 interfaces, etc.) to again provide the potential for volume production savings. Also, as the storage die design is suitable to be co-packaged with multiple storage die, the composite device formed by, for example, a 5-die stack (one interface die plus four storage die) design could be achieved that mimics a very high density DRAM device currently unachievable in the storage die's fabrication technology (e.g., a 4 Gb composite DRAM device can be constructed using DRAM die built in a 1 Gb DRAM fabrication technology). Also, as the storage die can be independently accessed, multiple storage die can be simultaneously activated to provide sufficient "core bandwidth" to meet the needs of the interface die's external "I/O bandwidth" requirements (e.g., two storage-die, each with maximum per-die bandwidth of 1.6 GBps, can be combined with an interface die to form a composite memory device that delivers 3.2 GBps externally). Also, the same storage die design can be packaged together with a highly integrated system-on-chip application-specific IC (such as a cell phone processor chip) which has particular memory requirements addressed by this storage die design (e.g., very low active power, simultaneous read/write access to different storage arrays, etc.).

FIG. **7**B illustrates an exemplary serializing circuit **320** that may be provided within an interface die to support configurable serialization of read data returned from a storage die within a multi-die memory device. Though not

specifically shown, a configurable deserializing circuit may be provided within the interface die to perform operations in reverse of those performed by the serializing circuit **320** and thus provide for read and write configurability of the high-speed interface data rate and data width. In serializing circuit **320**, a 32-bit portion (**322**) of a read data value (e.g., a 128-bit or larger column data value returned from a storage device), including bytes a0-a3, is latched within a first-stage storage buffer **321** in response to clock signal, ClkA. Byte pairs a0/a1 and a2/a3 are supplied to respective input ports of multiplexer **323** which responds to the level of ClkA (high or low in a given half clock cycle) to pass byte pairs a0/a1 and a2/a3 alternately to a second stage, two-byte storage buffer **325**. The second stage buffer **325** stores the byte pair forwarded in a given half cycle of ClkA in response to a clock signal, ClkB. ClkB oscillates at twice the frequency of ClkA so that both two-byte portions of the four-byte input **322** are stored per ClkA cycle. The two bytes stored within the second stage buffer, b0 and b1, are output to respective input ports of another multiplexer **327**, which in turn responds to the level of ClkB to pass bytes b0 and b1 alternately to a third stage, single-byte storage buffer **329**. The third stage buffer **329** stores the byte forwarded in a given half-cycle of ClkB in response to a clock signal, ClkC, having twice the frequency of ClkB so that all four of the originally received bytes a0, a1, a2 and a3 are stored in third stage buffer **329** in successive quarter-cycles of ClkA. As shown, the output of the third stage buffer **329** is provided, along with bytes b0 and a0 to respective input ports of output multiplexer **331**, which receives a 2-bit interface select signal ISel[1:0] at a control input. Bytes b1 and a1 are similarly provided to respective input ports of output multiplexer **333** which also receives the interface select signal. By this arrangement, the setting of the interface select signal (which may be configured through run-time program control, production-time setting and/or input-signal control as described above) may be used to select c0, b0 or a0 to be output via byte transmitter $\mathbf{341}_1$ and may similarly select bytes b1 or a1 to be output via byte transmitter $\mathbf{341}_2$. Transmitters $\mathbf{341}_3$ and $\mathbf{341}_4$ are used to drive bytes a2 and a3, when used in a given interface configuration. As shown, transmitter $\mathbf{341}_1$ is clocked by transmit clock tClk**1**, transmitter $\mathbf{341}_2$ is clocked by transmit clock tClk**2**, and transmitters $\mathbf{341}_3$ and $\mathbf{341}_4$ are clocked by transmit clock tClk**3**. In this arrangement, each of the four byte transmitters $\mathbf{341}_1$-$\mathbf{341}_4$ is enabled to output a respective byte of a 32-bit output data value when the interface select signal indicates a ×32, 1.6 Gb/s data interface. By contrast, when the interface select signal indicates a ×16, 3.2 Gb/s data interface, byte transmitters $\mathbf{341}_1$ and $\mathbf{341}_2$ alone are enabled to output data, 3.2 Gb/s data interface and, when the interface select signal indicates a ×8, 6.4 Gb/s data interface, byte transmitter $\mathbf{341}_1$ alone is used to output data. Table 340 shows exemplary clock rates, and the interface width and data rate for given values of the interface-select value. For example, if the interface select is set to '00', a ×8 data width and 6.4 Gb/s data rate are selected, in which case, ClkC oscillates at 6.4 GHz (6.4 G), ClkB oscillates at half that rate (3.2 G) and ClkA oscillates at half the clock B rate (1.6 G). Accordingly, a 32-bit data value **322** is loaded into the first stage buffer **321** every 625 nanoseconds (ns), with byte pairs a0/a1 and then a2/a3 being shifted into second stage buffer **325** in successive halves of the 625 ns input data interval, and finally with bytes a0, a1, a2 and then a3 being shifted into third stage buffer **329** in successive quarters of the 625 ns interval. Accordingly, transmit clock, tClk**1** oscillates at 6.4 GHz to enable byte transmitter $\mathbf{341}_1$ to transmit each byte of the four-byte sequence delivered via port '00' of output multiplexer at a 6.4 GHz data rate. Because byte transmitters $\mathbf{341}_2$-$\mathbf{341}_4$ are unused in ×8@6.4 Gb/s mode, transmit clocks tClk**2** and tClk**3** may be disabled and thus are shown in table 340 as "off."

When a 16-bit data width at 3.2 Gb/s is selected (ISel[1:0]=01), third stage buffer **329** is unused and ClkC may be disabled as shown, while ClkA and ClkB continue to oscillate at 1.6 GHz and 3.2 GHz, respectively. In this arrangement, a 32-bit data value **322** is loaded into the first stage buffer in each 625 ns input data interval (i.e., while read data is being output), with byte pairs a0/a1 and then a2/a3 being shifted into second stage buffer in successive halves of the 625 ns input data interval, and delivered via the '01' ports of output multiplexers **331** and **333** to byte transmitters $\mathbf{341}_1$ and $\mathbf{341}_2$. As shown, transmit clocks tClk**1** and tClk**2** are both operated at 3.2 GHz to transmit each pair of bytes b0/b1 every 312.5 ns. Transmit clock tClk**3** may remain disabled as byte transmitters $\mathbf{341}_3$ and $\mathbf{341}_4$ are unused in ×16@3.2 Gb/s mode.

When a 32-bit data width at 1.6 Gb/s is selected (ISel[1:0]=10), both the second and third stage buffers are unused and ClkB and ClkC may be disabled as shown. ClkA oscillates at 1.6 GHz to load a new 32-bit data value **322** into first stage buffer **321** every 625 ns. Bytes a0 and a1 are delivered to byte transmitters $\mathbf{341}_1$ and $\mathbf{341}_2$ via the '10' ports of output multiplexers **331** and **333**, and bytes a2 and a3 are supplied to byte transmitters $\mathbf{341}_3$ and $\mathbf{341}_4$. Transmit clocks tClk**1**-tClk**4** are operated at 1.6 GHz to establish the 1.6 Gb/s data transmission rate.

FIG. **8** illustrates an alternative embodiment of a multi-die memory device **400** having multiple storage dice $\mathbf{402}_1$-$\mathbf{402}_N$ coupled to a shared interface die **401**. In the embodiment shown, each of the storage die **402** has an asynchronous (i.e., un-clocked or clockless) control interface as discussed above and thus consumes substantially less static power than conventional integrated circuit memory die that include on-chip high-speed synchronous interface circuitry. Accordingly, storage capacity within the multi-die module **400** may be increased multi-fold without corresponding multiplication of the overall device power consumption. In one embodiment, each of the memory control interfaces $\mathbf{403}_1$-$\mathbf{403}_4$ within the interface die **401** is coupled via a multi-drop control/data signal path **405** a respective storage array within each of the storage dice $\mathbf{402}_1$-$\mathbf{402}_N$. Additional device-select control signals may be generated within the interface die **401** (e.g., based on address information received via high-speed interface **407**) to select one of the memory dice $\mathbf{402}_1$-$\mathbf{402}_N$ to respond to memory control signals on a shared path **405** during a given interval. Also, accesses to the memory dice **402** may be pipelined according to the deterministic data output times of the individual die **402** so that row operations (e.g., activation and precharge operations) may be performed in one or more of the memory dice **402** concurrently with column access operations (read or write operations) on one or more others of the memory dice **402**. Also, instead of shared data and control signal paths **405**, each of the storage arrays within each of the dice **402** may be coupled to the interface die **401** by a dedicated data path and/or control path.

FIG. **9** illustrates an alternative embodiment of a multi-die memory device **412** in which an interface die **415** includes a dedicated set of data interfaces for each storage die $\mathbf{416}_1$-$\mathbf{416}_N$. In the particular embodiment shown, for example, each storage die **416** includes four storage arrays (Q1-Q4), with like numbered storage arrays coupled via respective point-to-point (i.e., dedicated two transmission

between two endpoints as opposed to multi-drop) data paths **418** to corresponding dedicated data interfaces within control ports $\mathbf{417}_1$-$\mathbf{417}_4$ of the interface die **415**. More specifically, the Q1 storage array within each of memory devices $\mathbf{416}_1$-$\mathbf{416}_N$ is coupled via a respective point-to-point data path **418** to a respective data interface within control port $\mathbf{417}_1$ of the interface die, and the Q2-Q4 storage arrays are likewise coupled to respective data interfaces within each of control ports $\mathbf{417}_2$-$\mathbf{417}_4$. Although not specifically shown in FIGS. **8** and **9**, control signals (including row and column control signals, and row and column address values) may be communicated either asynchronously or in conjunction with a command timing signal (such as a clock or strobe signal) to each of the storage arrays via a dedicated point-to-point control path (i.e., control path per storage array), or via a multi-drop control path shared among all of the storage arrays, or via one of several multi-drop control paths that are shared by respective subsets of the storage arrays.

In one embodiment the total number of signaling interconnects (wires or other conductive structures) required to provide the point-to-point signaling paths **418** between the interface die and the DRAM die shown in FIG. **9** is reduced by time-multiplexing data transfer over the signaling paths. While this can be done in a straightforward manner for the unidirectional command and control interface (e.g., by using a conventional RAS/CAS DRAM control protocol), this presents particular challenges in the asynchronous storage dice **416** of FIG. **9** as there is no ready timing reference available to time the multiplexed, bidirectional data transfer. That is, in contrast to conventional synchronous storage devices which receive a free-running clock signal (and thus may output data and, in some cases, corresponding timing strobe signals in synchronism with the clock signal), a free-running clock is purposely omitted in the storage dice **416** of FIG. **9** to avoid power consumption during periods in which the storage dice **416** are not outputting data. In one embodiment, described in greater detail below, each of the storage dice **416** includes circuitry to output time-multiplexed read data in response to a signal, referred to herein as a demand signal, supplied by the interface die **415**. That is, after issuing a data read command directed to a given storage array (or set of storage arrays), the interface die **415** delays a predetermined time that corresponds to the time required for the requested read data to be retrieved from the array core, and then issues, via one or more signal paths, a sequence of demand signals to enable the storage array to responsively output a corresponding sequence of data chunks (or segments or components) that collectively form the requested read data word. By enabling the storage die data driver circuits only in response to assertion of the demand signal, time-multiplexed data transmission may be achieved with substantially reduced power relative to embodiments in which a free-running timing source is provided to (or generated within) the storage die. In effect, substantial transmission-related power consumption occurs only when data is demanded by the interface die **415**, rather than continually as in free-running clock embodiments.

FIG. **10** illustrates an embodiment of a multi-die memory device **420** in which an interface die **421** outputs a k-bit demand signal to a selected one of multiple storage dice $\mathbf{423}_1$-$\mathbf{423}_N$ (or at least one such storage die) to enable read-data output. More specifically, the selected storage die **423** responds to incoming memory access requests (command/control signals) by carrying out the requested memory access within a storage core **424**, then buffering the data for transfer in a data input/output (I/O) circuit **425**. The buffered data may then be output in a stream of component values referred to herein as data units, with each data unit being transmitted in response to a respective edge of the demand signal. By this arrangement, all timing control and related circuitry may remain on the interface die **421**, enabling the storage die **423** to be constructed simply and without power-consuming clocking circuitry, and yet the storage die **423** may still output data at rates that rival those of modern synchronous memory devices. As shown, the interface die **421** issues control signals to a selected one of storage dice $\mathbf{423}_1$-$\mathbf{423}_N$ via command/control path **426**, transfers data to and receives data from a selected storage die via data path **427** and issues demand signals to the selected storage die via demand path **428** (which may be a single signaling link). In one embodiment, the command/control path **426** may be coupled in multi-drop fashion to each of the storage dice $\mathbf{423}_1$-$\mathbf{423}_N$, while dedicated, point-to-point data paths **427** and corresponding demand paths **428** are provided between the interface die **421** and each storage die **423**. In alternative embodiments, point-to-point command/control paths **426** (or some portion thereof) may be provided between the interface die **421** and each storage die **423**, and/or multi-drop paths may be used for data and/or demand signal transfer. Also, individual data paths **427**, demand paths **428** and/or command/control paths **426** may be shared by subsets of devices, thus establishing a limited number of communication endpoints for each signaling path.

FIG. **11** illustrates an embodiment of a timing arrangement for bi-directional data transmission between storage die **423** and interface die **421** via data path **427**. Referring first to data transmission from interface die **421** to storage die **423** (e.g., write data transmission), a timing signal (T) generated (or received) within the interface die **421** is supplied to a transmit circuit **433** which responds to edges in the timing signal by transmitting individual write data units via data path **427**. The timing signal is supplied to (and propagates through) delay element D**1**, driven onto demand path **428** by demand-line driver **429**, and then received within storage die **423** and supplied to data receiver **431** to time the sampling of the write-data units conveyed on data path **427**. In one embodiment, the data receiver **431** performs a deserializing function by combining a sequence of n-bit data units received in response to edges of the timing signal into an m-bit received data value, R×D (m being greater than n). Delay element D**1** may be calibrated at production time, device initialization time and/or adaptively during device operation to align transitions in the timing signal as received at the input of the data receiver **431** with a desired sampling point (e.g., data eye midpoint) for the data waveforms conveyed via path **427**.

Still referring to FIG. **11**, an m-bit read data value (T×D) is supplied to data transmitter **430** which, in turn, transmits a sequence of n-bit data units (each being a component of the m-bit read data value) onto data path **427** in response to a respective edge of a k-bit demand signal conveyed on demand path **428**. That is, the interface die **421** outputs a demand signal to the storage die **423** and thus provides a timing reference for initiating data transmission within the storage die, effectively demanding each data-unit transmission. In the embodiment shown, the timing signal T propagates through delay element D**1** (though D**1** may be bypassed for demand signaling operation) and is driven onto demand line **428** by demand line driver **429**, thus effecting demand signal transmission. The demand signal is supplied to data transmitter **430** within the storage die **423**, with each transition of the demand signal (e.g., each high-to-low transition and/or low-to-high transition) used to trigger transmission of a respective data unit within the set of read

data units that constitute the read data value T×D. In one embodiment, the delayed timing signal output from delay element D1 is supplied to a second delay element D2 to yield a sampling signal (S) that triggers sampling operations within data receiver **432** to sample the read data units output by storage-die data transmitter **430**. As with D1, delay element D2 may be calibrated at production time, device initialization time and/or adaptively during device operation to align transitions in the sampling signal at the input of the data receiver **432** with a desired sampling point (e.g., data eye midpoint) for the data waveforms conveyed via path **427**.

In one embodiment, the storage die **423** includes control circuitry, not shown, to enable operation of data receiver **431** and data transmitter **430** at different times according to command/control signals received from the interface die **421**. For example, the control circuitry may enable the data receiver **431** to receive data in response to a timing signal conveyed via demand line **428** after receiving a data write command, and disable operation of the data transmitter **430** during the same interval. Similarly, the control circuitry may enable the data transmitter **430** to transmit data in response to demand signal transitions after receiving a data read command, disabling operation of the data receiver **431** during the same interval. On the interface die **421**, similar control circuitry, responsive to read and write commands from a memory controller, may alternately enable the data transmitter **433** and data receiver **432** to carry out the requested data transfer operations. In alternative embodiments, rather than re-use the existing data and demand signal paths, separate timing signal paths may be provided for write data timing (e.g., a data strobe path to convey a source-synchronous data strobe signal) than are used for the demand signal associated with read data timing. Also, the particular delay element configuration and timing signal timing may be different from that shown in FIG. **11** and established by virtually any circuitry within the interface die **421** and/or storage die **423** that is capable of adjusting the phase of the outgoing timing signals (or timing signal used to initiate interface-die data reception or transmission) relative to data transmit intervals via path **427**. Also, while the demand signal may consist of a single electrical signal with an oscillation frequency of the desired serialized data rate, it may also be realized by two or more phase-offset signals, which are combined within the output multiplexer circuit of the storage die to achieve the serialized data rate. Further, as shown in FIGS. **10** and **11**, as many as k demand signals may be asserted to initiate transmission of n data values, where k ranges from one to n. In one embodiment, for example, the ratio of n:k is 8:1, such that one demand signal is asserted for each byte of data transmitted during a given transmission interval. Other ratios of n:k may be used in alternative embodiments.

FIG. **12** illustrates a more detailed embodiment of a multi-die memory device **425** in which a demand signal is used to effect time-multiplexed read data transfer between an interface die **430** and a storage die **431**. Circuitry similar to that described in reference to FIG. **11** for timing and effecting write data transmission may be included within the interface die **430** and storage die **431** but, to avoid obscuring the read data path, is not shown. The interface die **430** includes a command decoder **433**, scheduler **435**, command/address register **437** (CA Reg), timer **439**, demand sequencer **441** (Dem Seq) and delay element **443** (all of which may be included, for example, within the command decode logic **131** shown in FIG. **2**) as well as a data receiver **445** which samples incoming read data in response to a sampling signal **444** (i.e., a delayed version of demand signal **434**) supplied by the delay element **443**. The storage die **431**, which may be the sole storage die or one of multiple storage dice within a multi-die memory device, includes command decode logic **457** (Cmd Decode) to receive command and address information from the interface die via command/address path **446**, and a data transmitter **459** (DQ Tx) to output read data to the interface die via data path **448** and in response to the demand signal **434** when driven onto demand path **450** (DEM) by driver **442**. Note that the interface die **430** and storage die **431** both may include additional circuitry (not shown) to support data write transactions, configuration operations and any of the various other operations described above.

The command decoder **433** responds to memory access commands (or requests) received via host command path **432** by generating corresponding memory access commands and address values that are queued for transmission in command/address register **437** and eventually driven onto command/address path **446** by command/address driver **438**. The command decoder **433** also signals the scheduler **435** to indicate command receipt and the nature of the command (e.g., read, write, configure, etc.) and thus enables the scheduler **435** to make decisions regarding the order and timing of command/data transmission to the storage die **431** and data receipt from the storage die. In particular, when a receipt of a memory read command is signaled by the command decoder **433**, the scheduler **435** asserts a launch signal **436** after an appropriate time delay (which time delay may depend, for example, on previously issued commands the transactions for which are in progress) to advance the memory read command to the head of the command/address queue (i.e, within the command/address register **437**) and enable the memory read command and corresponding address to be output via the command address path **446**. As discussed, the command and address may be output concurrently via respective portions of the command/address path **446** or in two or more time-multiplexed transfers over the command/address path.

In the embodiment shown, the launch signal **436** is also supplied to the timer **439** which delays for a predetermined time that is set or calibrated to the elapsed time between receipt of the memory read command within the storage die **431** and output of corresponding read data from the storage array **455** within the storage die **431**. After the predetermined time has elapsed, the timer **439** asserts a demand-enable signal **440** to enable the demand sequencer **441** to issue a sequence of demand signals **434**. The demand signals **434** are supplied to the data transmission circuitry **459** of the storage die (i.e., via demand-strobe line **450**) to enable transmission of a sequence of read data chunks and thus effect time-multiplexed output of a read data word **460** retrieved from the storage array **455** in response to the memory read command. The demand signals **434** are also supplied to the delay element **443** which generates, in response, a sequence of sampling signals **444** that are time delayed relative to the demand signals **434** according to the elapsed time between output of the first demand signal in the sequence and arrival of the first read data chunk at the data receiver **445**. The sampling signals **444** are supplied to the data receiver **445** as shown to sample the incoming sequence of read data chunks and thus receive the read data word output from the storage array **455** in response to the memory read command. After the sequence of read data chunks has been received, the demand signal **434** may be held at a steady-state (e.g., parked at a high or low level or at a midpoint between high and low levels) until another read

data transfer is to be effected, thus avoiding unnecessary state changes within the storage die **431** (i.e., as would occur in the case of a free-running clock signal or other continually toggling timing source) and conserving power.

FIG. **13** illustrates an exemplary memory-read command sequence and corresponding read data transfer sequence within the multi-die memory device of FIG. **12**. As shown, a memory read transaction is initiated when a read command **475** (COM) is received via the host command path **432** in FIG. **12**. Unless the read command is directed to an already activated storage row within the storage die, a row activation command **477** is issued to the storage die via command/address path **446** in response to the read command from the host. If the read command is directed to an already activated storage row, the activation command may be omitted. In one embodiment, the row activation command **477** includes a row address strobe (RAS) signal (and is thus also referred to herein as a RAS command) and may additionally include a row address, deasserted write enable signal and any other signals for specifying a row activation. A predetermined time, tRC (i.e., a row activation time specified for the storage array), after issuance of the row activation command **477**, a column read command **479** is issued to the storage die via the command/address path **446**. In one embodiment, the column read command **479** includes a column address strobe (CAS) signal (and is thus also referred to herein as a CAS command) and may additionally include a column address, deasserted write-enable signal and any other signals for specifying a column read command. A first predetermined time after issuance of the column read command, tCC (i.e., a memory core timing constraint specified for the storage die), a second column read command **481** directed to a different column address within the activated row of data may be issued via command/address path **446** to initiate a second read operation. Also, referring to FIGS. **12** and **13**, a second predetermined time after issuance of the column read command **479** (which may be the same as or longer or shorter than tCC), a read data word **460** becomes valid at an output of the storage array **455** and therefore available to be latched within the data transmitter **459** and output from the storage die. As shown, the timer **439** within the interface die **430** is set or calibrated to assert the strobe-enable signal **440** at a time such that an initial rising edge of the demand signal edge (i.e., a first demand signal assertion) arrives at the data transmitter **459** of the storage die **531** shortly after (or coincidentally with) valid data output from the storage array **455**. In one embodiment, the initial demand signal edge within a sequence or burst of demand signal edges latches the read data word **460** present at the output of storage array **455** within a word latch circuit of the data transmitter **459** and also enables a selected chunk of the data word to be driven onto data path **448**. Subsequent demand signal assertions, including falling-edges and rising edges of the demand signal are used to select remaining chunks of the data word to be driven onto data path **448** in sequence (i.e., one after another) as shown at **480**, thereby effecting time-multiplexed transmission of the entire read data word **460**. In the particular example shown, eight chunks of read data, numbered 0-7, are transmitted in succession (effecting an 8-chunk data burst) in response to eight transitions of the demand signal to effect time-multiplexed transmission of the read data word **460**. More or fewer demand signal transitions may be generated by the demand sequencer **441** in alternative embodiments to achieve smaller or larger burst lengths (i.e., more or fewer chunks per read data word transmission) or serialization ratios. Also, the burst length may be established by a one-time or reconfigurable setting within the interface die **430** (e.g., a programmable register setting). Further, while rising and falling edges of the demand signal are depicted as triggering data chunk output at the storage die, rising edges only or falling edges only may be used to trigger data chunk output in alternative embodiments. Also, while the demand signal is shown in FIG. **12** as a single electrical signal with an oscillation frequency of the desired serialized data rate, it may also be realized by two or more phase-offset signals, which are combined within the output multiplexer circuit of the storage die to achieve the serialized data rate.

Still referring to FIG. **12**, the second CAS command **481** results in assertion of an additional demand signal sequence and corresponding 8-chunk output data burst as shown at **482**. Additional CAS commands may be issued to effect additional back-to-back output data bursts. Also, as shown at **483** (during intervals in which no read data is to be transmitted), the demand signal may be parked at a logic low or high level to disable latching and data transmission operations within the storage die. The demand signal may also be parked at midpoint or other level between the logic low and high levels and, if desired or necessary, a preamble and/or postamble protocol established to indicate transmit-enable edges (i.e., edges that are used to enable latching and/or transmission operations within the storage die).

As discussed above, the sampling signal **444** (Samp) output by the delay element **443** is a time-shifted version of the demand signal, delayed according to the time required for data to propagate through the storage die output circuitry (i.e., data transmitter **459**) and across the data path **448** to the data receiver **445**. The delay of the sampling signal relative to the demand signal may also include a quadrature delay component to establish the sampling signal transition at the midpoint of incoming data eyes as shown at **484**, thus ensuring that each data chunk conveyed in the incoming data signal is sampled during a data valid interval. Techniques for calibrating the delay element **443** to provide a desired timing relationship between the sampling signal **444** and incoming data are discussed below.

FIG. **14** illustrates an embodiment of a data transmit circuit **501** (DQ Tx) that may be used to implement data transmitter **459** of FIG. **12** and its interconnection to a storage array **503** and demand path **450**. In one embodiment, the command decoder within the storage die generates a control signal **504** (Cntrl) in response to each CAS command after allowing any ongoing output data burst from a preceding CAS command to be completed. The control signal **504** is supplied to an asynchronous reset input (R) of a flip-flop **505** or other bi-stable device to lower a latch enable signal **506** (the flip-flop output) and thus a transparent mode (i.e., data flow-through) in latch **507**. By this operation, when a READ data word **502** (depicted as a 64-bit value in the embodiment of FIG. **14**, though larger or smaller data words may be output from the storage array) becomes valid at the output of storage array **503**, the data word flows through the latch to the input of serializer **509**. In the particular embodiment shown, the demand path **450** is coupled to the clock input of flip-flop **505** and to serializer **509**. The data input of the flip-flip **505** is tied high so that, at the initial rising edge of a sequence of demand signal transitions, the flip-flop drives latch-enable signal **506** high to latch the read data word **502** within the transparent latch, thus maintaining availability of the read data word **502** for time-multiplexed transmission and at the same time enabling a subsequent memory transaction (e.g., a pipelined memory read or write operation) to be carried out within the storage array **503**.

Still referring to FIG. **14**, the serializer **509** performs a parallel-load, serial-shift function, enabling each of multiple chunks of the latched data word (i.e., read data word within latch **507**) to be output onto the external data path **448** (e.g., by output driver **512**) in succession to effect time-multiplexed transfer of the entire read data word. In the implementation shown, the serialization data rate (i.e., relative to a system clock source, not shown) is controlled by the demand signal rate, and not by a timing signal synthesized by the storage die. In the particular embodiment shown, the serializer **509** supplies a sequence of eight byte-size data chunks (i.e., 8-bit values) to eight output drivers (collectively designated **512**) in response to rising and falling edges of demand signals on each of four demand signal lines within demand path **450**. For example, each of the output drivers **512** may receive a respective one of the four demand signals and, on each transition of the demand signal (i.e., each rising edge and each falling edge), the output driver transmits a bit onto a respective line of data path **448**. By this operation, after eight transitions on each of the four demand signals, the entire 64-bit input word has been transmitted from the storage die to the interface die, where the actual data rate of that transmission is controlled by the interface die (i.e., by establishing the toggling rate of the demand signals). Note that longer or shorter burst lengths of differently sized chunks may be output in accordance with application requirements (e.g., chunk size may be programmed within the storage die and/or burst length may be programmed within the interface die). Also, though not specifically shown, the output drivers **512** may be enabled by assertion of the latch-enable signal (or a delayed version thereof) and tri-stated at other times to enable bi-directional data transfer over the external data path **448**. Also, the output drivers **512** may be integrated within the serializer **509** in alternative embodiments, as where multiple output drivers are enabled in succession to drive respective chunks of the latched data word onto the external data path. Also, as described previously, the demand signal as provided by the interface die to each output driver may consist of a single signal with a transition frequency at the desired serialized data rate, or it may consist of two or more phase-offset signals which collectively provide phase-offset transitions that correspond to the desired serialized data rate.

FIG. **15** illustrates an alternative embodiment of a serializer **523** and latch **521** that may be used to implement the serializer **509** and latch **507** of FIG. **14**. Latch **521** includes a parallel input **522** to receive a 64-bit data word from a storage array (larger or smaller data words may be latched in alternative embodiments) and latches the data word in response to a high-going latch-enable signal (not shown). Latch **521** outputs eight data bytes (8-bit chunks) B**0**-B**7** in parallel to the serializer **523** (as discussed there may be more or fewer chunks each having more or fewer constituent bits). The serializer **523** includes a multiplexer **525** and control circuit **527** (MuxCntrl) which cooperate to output each of the input data bytes in turn to each of the driver circuits or, if the multiplexer includes driver circuitry, onto an external signal path. In one embodiment, for example, the control circuit **527** responds to an initial transition of the demand signal by enabling a first output driver within multiplexer **525** to output byte B**0** onto the external signal path, and then to a subsequent transition of the demand signal by disabling (e.g., tri-stating) the first output driver and enabling a second output driver within multiplexer **525** to output byte B**1** onto the external signal path. Thereafter, subsequent transitions of the demand signal result in like disabling of the currently active output driver and enabling of the output driver for the next byte in the data transmission sequence. The individual output drivers may be coupled in a wired-OR to the output contact. In an alternative embodiment, the control circuit **527** may issue a sequence of multiplexer control signals to the multiplexer **525** to switchably pass each of the input bytes, in sequence, to a shared output driver (not shown in FIG. **15**) for transmission in successive time intervals. In one embodiment, multiplexer **525** is implemented by a pulsed signaling multiplexer as described in greater detail below.

As discussed in reference to FIG. **12**, a timing calibration may be performed to enable the interface die to determine the appropriate time delay between assertion of a demand signal and assertion of a corresponding sampling signal to sample the read data value output in response to the demand signal. FIGS. **16**A and **16**B illustrate an exemplary timing calibration operation that may be carried out by the interface die **430** of FIG. **12** to determine an appropriate time delay between assertion of demand signal **434** and assertion of read data sampling signal **444**. In general, the approach of FIGS. **16**A and **16**B involves sweeping the delay setting (and thus the propagation delay) of delay element **443** through a sequence of delays to identify a range of delay settings within which data may be reliably read from the storage die **431** and then establishing a desired timing offset at the midpoint within the range. In one embodiment, a known data pattern is read from the storage die **431** (e.g., from a pre-loaded register, a hardwired test value, or pre-loaded location within the storage array **455**) and compared with the expected value to determine a pass or fail result for each delay setting. Referring to FIG. **16**A, then, at **551** a minimum timing offset (i.e., delay setting) is established within the delay element, and then the known data pattern is read at **553**. The read data is compared with expected data in decision block **555** and, if no match is detected, the timing offset is advanced at **557** and the data read and compare operations at **553** and **555** are repeated. Note that the data read operation at **553** may involve numerous reads to ensure that, if a match is detected, the match is not a statistical aberration or that the timing offset is so near the edge of the desired range that one or more subsequent data reads at the same timing offset will yield failing results.

Referring to FIGS. **16**A and **16**B, the timing offset is iteratively advanced from the minimum timing offset **579** until, when a data match is finally detected at decision block **555**, a lower timing offset is reached **571**. At this point, the lower timing offset is recorded in a temporary register at **559**, the timing offset is advanced at **561** and data read and compare operations **563** and **565** are performed to determine whether an upper timing offset has been reached. That is, if a data mismatch is not detected at **565**, then the timing offset is deemed to remain in the passing range (between lower timing offset **571** and upper timing offset **572** as shown in FIG. **16**B) and the timing advance, data read and compare operations (**561**, **563**, **565**) are repeated iteratively until a data mismatch (i.e., failing result) is detected. When a data mismatch is detected, the timing offset applied just prior to the mismatch detection (i.e., the most advanced timing offset at which no data mismatch occurred) is recorded as the upper timing offset at **567**, and then a final desired timing offset is determined at **569** based on the upper and lower timing offsets. In the particular embodiment shown, for example, the upper and lower timing offsets are averaged to determine a desired timing offset **575** at the midpoint of the passing range (e.g., as shown in FIG. **16**B), though the upper and lower timing offsets may be applied in various alternative ways to establish desired timing offsets that are advanced or delayed relative to the midpoint of the passing

range. In any case, after the desired timing offset is determined, the desired timing offset is applied within the delay element **443** to control the delay between outgoing demand signal edges and corresponding edges of the receive data sampling signal.

Depending on the system timing margin, the calibration operation of FIGS. **16**A and **16**B may be performed during system production to establish a one-time programmed delay value, or may be performed one or more times during device run-time to establish a dynamically controlled delay value. For example, in one embodiment, the calibration operation may be performed at device startup to establish the desired timing offset, and then left alone thereafter or repeated periodically or in response to certain events. In a particular implementation, for instance, the calibration operation may be carried out as frequently as necessary to compensate for temperature and voltage-induced timing drift and/or may be performed concurrently with refresh operations or other maintenance operations within the storage die. Also, while a linear search has been described (i.e., stepping the timing offset incrementally through a range of values), various alternative approaches for determining a desired timing offset may be applied, including binary or other non-linear searches, coarse/fine searches (i.e., coarse-stepping of the timing offset to identify the pass/fail boundaries at either end of the passing range, followed by fine-stepping of the timing offset within the coarse steps across the boundaries), and techniques that seek to minimize bit error rate or optimize other statistical results. Also, while calibration of the delay imposed by delay element **443** has been described, similar calibration operations may be carried out to determine the time delay imposed by timer **439** (i.e., how long to wait before asserting strobe-enable signal **440**) or any other timing-dependent operations within the multi-die memory device. For example, the storage die **438** may contain a "feedback path" transmitter circuit, representative of the storage die's other transmitter circuits, which the interface die **430** can utilize within a closed-loop timing system to calibrate the required delay of delay-element **443**. In other embodiments, to minimize the amount of timing calibration circuitry, the calibrated delay value for one chip-to-chip interface can be simultaneously applied to several other like chip-to-chip interfaces.

In multi-die memory device embodiments described thus far, the interface die is used to control timing and data access operations within one or more storage die. In those embodiments and others discussed below, the interface die may additionally include circuitry to control various other operational aspects of the storage die. Referring to FIG. **17**A, for example, an interface die **601** may include a variable-output voltage regulator **605** (Signaling Voltage Regulator) to provide one or more supply voltages to output drivers within the storage die **603** and thus control the amplitude of output signals generated by the storage die **603**. In the particular embodiment shown, the interface die **601** generates a supply voltage, V_{SWING}, which is provided to the storage die through contact **608** (or other interconnect structure) and used to power output driver **609**, thereby enabling output driver **609** to generate waveforms having amplitudes determined by the interface die as shown in FIG. **17**B (i.e., V_{SWING} may be set to any of voltages V_1-V_n to establish the output voltage swing impressed on line **612** via contact **610**). In alternative embodiments, the interface die **601** may generate both upper and lower voltages used to power the output driver **609**. Also, instead of providing a supply voltage, the interface die may source or sink a driver biasing current. Similarly, though an inverter-type output driver **609** is depicted, virtually any type of output driver may be powered by the interface die **601** including, for example and without limitation, differential or single-ended, current-mode or voltage-mode, AC-coupled or DC-coupled output drivers. In yet other embodiments, the interface die **601** may provide a control value that is supplied to one or more digital-to-analog converters (DACs) within the storage die **603** to generate one or more supply voltages or currents for controlling the common mode and/or signal swing of the storage die output drivers. The control value may be applied directly to the DAC(s) or may be stored within a programmable register or other configuration circuit within the storage die **603**. With regard to calibration, searching strategies similar to that described in reference to FIGS. **16**A and **16**B (including variations thereof) may be used to determine a desired current and/or voltage supply level. For example, the supply voltage and/or current may be stepped through a range to identify a threshold at which data is reliably received, and then set to the threshold (multiplied by a safety factor, if desired). Also, though only a single supply output is depicted, the interface die **601** may generate multiple supply outputs for respective storage dice **603**, or for output drivers associated with respective storage arrays within a given storage die, or even for individual output drivers or groups of output drivers associated with a given storage array.

To mitigate the "known good die" (KGD) problem (also known as the "compound yield" problem) generally associated with multi-die packages, the interface die within a multi-die memory device may also be used to control mapping of redundant rows and/or columns onto defective or suspect rows/columns of storage cells within a counterpart storage die. That is, in contrast to conventional techniques in which relatively large (and therefore expensive in terms of consumed die area) laser fuses or other one-time programmable structures are provided within a storage device to support production-time selection between a suspect row or column and a redundant counterpart, a much smaller programmable register or other run-time configurable structure may be provided within the storage die and loaded (i.e. programmed) with one or more redundancy control values at device startup. The redundancy information may be stored, for example, within a non-volatile storage circuit within the interface die or within another die (e.g., a separate non-volatile storage die within the multi-die package) that is coupled to provide the redundancy information to the interface die. Also, the storage die may receive the redundancy information in the form of control signals passed via the control interface (e.g., the interface used to issue row, column and other memory-related commands or requests) or via a separate interface. Referring to the embodiment of a multi-die memory device depicted in FIG. **18**, for example, interface die **640** may include a built-in-self-test (BIST) engine **645** to execute various self-tests directed to circuitry on the interface die **640** and on storage die **641** (e.g., pattern generation, pattern comparison, memory write/read/modify tests, retention tests and various other tests similar to those performed at wafer sort, burn-in, and final test in conventional memory devices), and thus may identify defective or unreliable rows and/or columns of storage cells within storage die **641**. In one embodiment, the BIST engine **645** issues programming instructions to the storage die (e.g., communicated by serial-port controller **647** to counterpart serial port controller **651** on the storage die **641**) to establish settings within programmable register **653** to control the selection (shown conceptually by multiplexer **655**) between defective/unreliable rows or columns (F) and

redundant rows or columns (R). Defective or unreliable rows/columns within the storage die **641** may alternatively (or additionally) be identified during device production test and mapping between such rows/columns and their redundant substitutes programmed within an optional e-fuse bank (or other non-volatile storage, including on a non-volatile storage die co-packaged along with the interface die and the storage-die) of the interface die **640**. In such an embodiment, the e-fuse redundancy mapping may be output to the storage die **641** at device startup (e.g., via serial port controllers **647** and **651**) to establish settings within register **653** to control redundant row/column selection. In other embodiments, defective row/column information identified during production test can be stored within computing equipment associated with the production test environment. This defective row/column information can then be used to determine redundancy maps which are loaded into the final composite device's non-volatile storage during or after final assembly. In one embodiment, the multiplexers associated with each row repair domain (e.g., there may be one redundant row for every megabyte of DRAM storage array) are connected in shift-register series, thus forming a "scan chain" arrangement. To assign a row redundancy control value, the interface die may "scan in" (or shift in) the desired value. A similar approach can be used to control column redundancy multiplexers. In any case, relatively large, production-time programmable structures such as laser fuses may be omitted from the storage die **641** (or at least reduced in number) without sacrificing yield-enhancing redundancy features (additionally, if the non-volatile storage is re-programmable, a failing DRAM device can potentially be repaired in the field). Accordingly, a larger percentage of the die area is available for implementing the storage array **657** (and/or for additional redundant rows and/or columns of storage cells), thus potentially reducing the per-bit cost of the storage die **641**.

FIG. **19** illustrates an embodiment of a multi-die memory device in which interface die **671** includes a power regulator **675** to selectively power each of multiple storage arrays $\mathbf{681}_1$-$\mathbf{681}_4$ within a storage die **673** (or multiple storage dice), thereby enabling unused storage arrays **681** to be switched off (i.e., powered down) to conserve power. In the embodiment shown, the interface die **671** includes an allocation map **677** that indicates which of the storage arrays **681** are in-use (i.e., used to store data) at a given time, and that outputs a set of enable signals **676** to the power regulator **675** to enable or disable power delivery to the storage arrays **681** accordingly. In one implementation, the allocation map **677** is cleared upon device power up, and then updated in response to host memory write commands. As memory write operations extend to each additional storage array **681** within storage die **673**, the allocation map asserts the corresponding enable signal **676** for the storage array to enable power delivery thereto. In one embodiment, the interface die **671** may additionally receive deallocation notices or information from the host processor (or memory controller or other control entity) and may power-down storage arrays **681** in which all previously allocated memory space has been deallocated and thus are no longer in-use.

Still referring to FIG. **19**, the allocation map **677** may indicate in-use regions of the storage die **673** with sufficient granularity to enable selective refreshing of storage rows therein. For example, in one embodiment, the allocation map **677** includes a number of array-map registers that correspond to respective storage arrays **681** within the storage die **673** (or storage dice), with each array-map register having a number of bits that correspond to respective rows of storage cells within the counterpart storage array. By this arrangement, individual bits of a given array-map register may be set or reset to indicate whether the corresponding storage row is in use (i.e., bits set or reset according to memory write requests and, if provided, deallocation notices from the host) and the in-use information **678** output to a refresh controller **679** to enable refresh operations to be bypassed for unused storage rows. Accordingly, refresh operations may be directed only to in-use storage rows, thereby saving power within the multi-die memory device relative to embodiments in which refresh operations are indiscriminately directed to all storage rows in sequence.

FIG. **20**A illustrates an exemplary packaging arrangement that may be used to encapsulate a pair of storage dice $\mathbf{702}_1$, $\mathbf{702}_2$ within a multi-die memory device **725**. As shown, the multi-die memory device **725** includes a module substrate **727** having conductive interconnection structures (e.g., traces, vias, etc.) generally as described in reference to FIGS. **6**A and **6**B. The interface die **701** and a first storage die $\mathbf{701}_1$ are disposed on the substrate **727** and coupled to one another as described above (e.g., via wire bond or flip-chip interconnects), and a second storage die $\mathbf{702}_2$ is disposed on top of the first storage die $\mathbf{702}_1$ to form a die stack. A cover or housing **728** may be disposed over the dice **701**, **702** and interconnection structures, and secured to the substrate **727**. Though not specifically shown, a dielectric spacer may be disposed between the first and second storage dice to isolate the die from one another. Also, in an embodiment in which the first storage die $\mathbf{702}_1$ is wire-bonded conductive interconnect structures in or on the module substrate **727**, the first and second dice **702** may be offset from one another as shown (i.e., offset from a centerline that extends through the stack and normal to the substrate) to expose edges of the dice **702** for wire-bond access. As shown in embodiment **730** of FIG. **20**B, additional storage dice $\mathbf{702}_2$-$\mathbf{702}_N$ may be added to the die stack (thus achieving a stack of dice $\mathbf{702}_1$-$\mathbf{702}_N$) and offset from one another to enable wire-bond access to each. A cover or housing **732** may be disposed over the interface die **735** and storage dice **702**, and secured to module substrate **736**.

FIG. **20**C illustrates another packaging embodiment **740** in which an interface die **745** and storage dice $\mathbf{702}_1$-$\mathbf{702}_N$ are disposed in separate integrated circuit packages **741**, **743** that mate to one another to form a multi-package module. In this approach, the external, electrical interface protocol (i.e. the DRAM "flavor") can be selected at final assembly by the memory module manufacturer, rather than during memory die fabrication by the DRAM vendor. Although a package-on-package implementation is shown, a package-in-package arrangement may be employed in alternative embodiments. Also, a single storage die **702** may be disposed within the storage die package **741** instead of multiple storage dice **702** as shown. Further, instead of staggering the storage dice **702** to enable wire-bond access, other interconnection schemes and/or die stacking arrangements (including, but not limited to, thru-silicon vias, flex-tape, die-in-substrate encapsulation, direct wafer bonding, proximity interconnect) may be used. The package-to-package interconnections **747** may be established by direct electrical contacts (e.g., ball grid array, micro-ball grid array, spring contacts, pad-to-pad contacts and the like), or by contactless interconnects such as capacitive or inductive interconnects.

FIG. **20**D illustrates yet another packaging embodiment **750** in which an interface die **755** is mounted in a flip-chip configuration with contact pads mated via micro-ball-grid array or other contact technology to counterpart landings on

a module substrate **753** and thereby interfaced (e.g., through traces on and/or within the module substrate **753**) to wire-bond interconnections to one or more storage dice **702**$_1$-**702**$_N$ stacked above the interface die **755**. The entire stacked die arrangement may be encapsulated within a housing **751**, molding or other protective structure.

FIG. **20**E illustrates a package-on-package (PoP) embodiment **760** having a storage package **762** stacked on an interface package **761**. The storage package **762** includes a substrate **763** having storage die **702**$_1$-**702**$_N$ stacked thereon and encapsulated within molding or housing **765** as generally described above. The interface package **761** includes an interface die **767** wire-bonded or flip-chip mounted (or otherwise coupled) to substrate **769** and encapsulated within molding or housing **764**. Solder balls **768** (or any other interconnection structures) may be used to form electrical contacts between the interface package **761** and storage package **762**.

FIG. **20**F illustrates an alternative embodiment of a package-on-package embodiment **770** having one or more storage packages **772**$_1$, **772**$_2$ stacked on an interface package **771**. In contrast to the embodiment of FIG. **20**E, an interface die **777** is mounted on the underside of a substrate **779** (and optionally encapsulated within housing or molding **773**) to form interface package **771**, and storage die **702**$_1$ is similarly mounted on the underside of substrate **7761** in storage package **772**$_1$. By this arrangement, lower profile interconnects **778** (e.g., micro-balls or other low-profile interconnects) may be used to electrically couple the first-level storage package **772**$_1$ to second-level storage package **772**$_2$ and thus reduce package height relative to a device having a stack of same-orientation storage packages **772**. One or more storage additional storage packages **772** (not shown) may be stacked on top of storage package **772**$_2$ to increase the overall package storage capacity. The storage packages **772** may be constructed generally as described in reference to FIG. **20**E, each having a substrate **776** and at least one storage die **702** (each or any of the storage packages **772** may have multiple storage dice as, for example, in the embodiment of FIG. **20**E) encapsulated within housing or molding **774**. In the embodiment shown, electrical interconnections between the interface package **771** and first-level storage package **772**$_1$ may be formed, for example and without limitation, by solder balls **775** or other contacts.

FIG. **21** illustrates an embodiment of a memory module **800** having rows of multi-die memory devices **801** disposed on front and rear faces of a substrate **803** (the devices on the rear face of the substrate being shown in dashed outline). Traces disposed on the substrate **803** (including traces on submerged layers of the substrate) are used to convey signals between an edge connector **804** of the module and the multi-die memory devices **801**. Because each of the multi-die memory devices **801** may be designed to mimic the operation of various conventional memory devices, the memory module **800** itself may be pin compatible with memory modules populated by conventional devices. Accordingly, the memory module **800** may be installed in connector sockets in place of conventional memory modules, for example to reduce power consumption and/or increase capacity within a memory system. Although eight multi-die memory devices **801** are shown on each face of the module **800**, more or fewer devices may be provided according to interface or data width demands. For example, a ninth memory device **801** may be provided within each row to store error correction code (ECC) or other error-detection/correction data for the contents of the remaining memory devices **801** in the row. Also, while not specifically shown, a non-volatile storage such as a serial-presence-detect (SPD) memory may be disposed on the memory module to store characterizing information regarding the multi-die memory devices, including their programmable functions (e.g., interface programmability as described above), storage capacity, data rate capability and so forth.

FIG. **22** illustrates a memory subsystem **850** that includes a memory controller **870** and a pair of multi-die memory devices **803**$_1$, **803**$_2$ disposed in a package-on-package arrangement. In the particular embodiment shown, each of the memory devices **803** includes an interface die **855** and a single storage die **857** disposed in a stack as generally shown in FIG. **20**D, though any of the multi-die memory device embodiments discussed above may alternatively be used, including those with multiple storage dice. Also, with respect to the package-on-package coupling via interconnects **861**, the multi-die memory device **803**$_2$ is disposed in an inverted arrangement to take advantage of the cavity formed by module-to-module interconnection solder balls **863** and thus reduce the overall height of the package-on-package memory subsystem **850**. The memory controller **570** includes a control logic die **864** that may be a dedicated memory controller, or an application specific integrated circuit (ASIC) that includes functions other than (or in addition to) memory control including, without limitation, cell phone baseband processor, graphics pipeline support, bus bridge, processor-local-bus interface and so forth. Alternatively, the memory controller **570** may be part of a general-purpose or special-purpose processor or controller. As shown, the memory controller **570** may also be disposed in an inverted configuration to take advantage of the cavity formed by module-to-circuit-board interconnection balls **865** and thus reduce the overall height of the package-on-package memory subsystem. Although not shown, a housing or other structure may be partially or completely formed or molded over the package-on-package arrangement of FIG. **22** to provide heat dissipation (cooling) and/or structural integrity.

In other embodiments, additional multi-die memory devices and/or other integrated circuit packages may be mounted in the package-on-package stack to provide additional memory capacity or other functionality. Also, while the interface die in the various embodiments described above has been described in terms of its function as an intermediary between one or more storage die and an external device such as a memory controller or processor or ASIC (application-specific integrated circuit) having a memory control function, the circuitry that constitutes the interface die may be implemented on the same die or in the same integrated circuit package as a memory controller, processor (e.g., a central processing unit, graphics processing unit, digital signal processing unit, etc.), ASIC or the like. As discussed, this allows potential cost savings to ASIC manufacturers by enabling a low-power DRAM design die design suitable for System-in-Package integration to also be shipped in high-volume, industry-standard DDR memory markets.

FIG. **23** illustrates an embodiment of a pulsed signaling multiplexer **870** that may be used to implement output multiplexers and/or serializing multiplexers in the various integrated circuit devices and systems described above, including multiplexer **525** within the data serializing circuit of FIG. **15**. As shown, multiplexer **870** includes timing circuitry **878** having a plurality of timing circuits **880***a-n* coupled to transmitter circuitry **872**. The transmitter circuitry includes an array of AC-coupled transmitter circuits **874***a-n* that generate pulsed output signals. A common

output node **876** receives the plurality of transmitter output signals in a time-multiplexed manner as more fully described below. By transmitting signals in this fashion, significant improvements in signal throughput and power efficiency for integrated circuits may be realized.

Still referring to FIG. **23**, the plurality of AC-coupled transmitters **874***a-n* may be disposed in a parallel configuration with respective outputs tied together to the common output node **876**. For purposes of clarity, only one transmitter **874***a* will be described in detail, it being understood that all of the transmitters may be substantially similar in construction. Each transmitter includes an amplifier circuit or driver **882** such as a CMOS inverter, for example. The output of the driver feeds an AC-coupling element such as a series capacitor **884** that includes an output terminal **886** for directing an AC output signal to the node **876**. Each series capacitor **884** may have a capacitance on the order of around 50-150 fF (femto-Farads), and may be manufacturable through standard CMOS fabrication techniques. Moreover, it should be understood that, depending on the application, the on-die AC-coupling element may comprise a portion of a series capacitor, that for example, may cooperate with another portion of a series capacitor at a receiver end, or as part of the package assembly process (e.g., by using redistribution layer metal to form the top plate of a capacitor) to effect an entire capacitor structure. This enables flexibility for chip-to-chip applications where, for example, the contactless interconnect between two adjacent integrated circuits may be a series capacitor structure. Other alternatives are available as well, such as inductors to effect inductive coupling between chips.

The timing circuitry **878** provides signal offsets for input to the plurality of transmitter circuits **874***a-n*. FIG. **24** illustrates one embodiment of the timing circuitry, generally designated **900**, for use with the transmitters described above. A plurality of flip-flops **902***a-n* are disposed at each transmitter input (not shown), and have respective data input lines **904***a-n* and demand lines **906***a-n* (collectively forming an N-bit demand path **909**) to receive independent data and demand signals. In one embodiment, a multi-phase clock generator or source **908** within interface die **907** outputs N demand signals on demand lines **906***a*-**906***n*, respectively, with the demand signals being offset in phase by desired phase increments. The phase offset demand signals are then fed to the clock inputs for the flip-flops **902***a*-**902***n* as shown. Suitable multi-phase clock generators may be realized, for example and without limitation, using simple delay lines, oscillator-fed delay-locked-loop (DLL) circuits, or phase-locked-loop (PLL) circuits, where offset clock signals may be tapped following each delay element in a delay line (for the DLL), or each element in a ring oscillator (for the PLL).

Alternatively, the timing circuitry **908** may comprise a plurality of programmable or variable delay elements (not shown) to offset data signals being input to the transmitter circuitry **872**. Static weighted delay elements might also be used to provide the different delays. Additionally, while the timing circuitry described above is implemented upstream of each AC-coupled transmitter input, similar benefits may be realized by employing the timing circuitry between the outputs of the drivers and the series capacitors.

Referring again to FIG. **23**, to maximize the bandwidth of the transmission channel, the multiplexer described above may employ termination circuitry **890** in the form of a termination resistor Rterm coupled between the node **876** and a termination voltage terminal Vterm (shown in this embodiment as DC ground). For applications involving relatively short transmission channel lengths, such as "system-in-package" (SiP) environments or other multi-component packages as discussed above, the termination resistor Rterm may be realized by an on-chip resistor implementation. The termination resistor may be realized through many different alternative embodiments, including single or multiple resistor implementations, transistor circuitry to effect a resistive output, and the like.

Due to the loading of multiple capacitive elements in parallel, the signal amplitude on node **876** generated by any one of the individual AC transmitters is reduced compared to how the transmitter would perform in isolation. However, due to the non-zero output impedance of the driver circuit **882**, the attenuation effect can be kept to reasonable levels. In an alternative embodiment, the output impedance of the driver circuit **882** may be increased, thereby decreasing the signal attenuation effect, by employing a tri-state driver in each transmitter **874**. Such drivers are configured to exhibit a high impedance output when operating in a non-driving mode.

In some applications, electrostatic discharge (ESD) protection circuitry **130** may be disposed in parallel with the termination resistor Rterm. The ESD circuitry may include a pair of reverse-biased diodes D**1** and D**2** tied between the node **876** and the termination voltage Vterm. Due to the AC-coupled natured of the pulsed signaling multiplexer **870**, the ESD circuit complexity may be minimized, which can substantially reduce DRAM die cost by reducing the die size overhead associated with the external interface system on the DRAM die.

In one embodiment, the pulsed signaling multiplexer **870** and its supporting circuitry may be realized by circuitry employed on a single integrated circuit. In other embodiments, one or more support circuits employed by the multiplexer may be implemented on a second integrated circuit.

In operation, data signals are fed along independent data paths to the timing circuitry **878**, where they are re-timed (or offset). The re-timing allows the multiplexer transmitters **874***a-n* to receive at their inputs data signals that are precisely offset in phase with respect to each other. FIG. **25** illustrates an example of the timing relationships between the input data fed from the timing circuitry to the AC-coupled transmitters **874***a-n*, and the combined output data pulse stream at the common node **876**.

As shown in FIG. **25**, each transmitter signal output may be offset by an incremental phase. Due to the high-pass filtering nature of the series capacitor, the transmitter output comprises a brief pulse corresponding to the rise and fall times of the input data edge transitions. Since only signal transitions appear at the output of each transmitter, pulses appear on the output node for each signal transition in an "wired-OR" manner. This, in effect, provides a dramatic increase in the signaling rate at the output node **876**. In one embodiment, where eight transmitters may be arrayed in parallel with a single output, and offset in phase by ⅛ a symbol period (half the multi-phase clock period), a very low power parallel-to-serial transmitter circuit is achievable.

It should be noted that the various integrated circuits, dice and packages disclosed herein may be described using computer aided design tools and expressed (or represented) as data and/or instructions embodied in various computer-readable media, in terms of their behavioral, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to, formats supporting behavioral languages such as C, Verilog, and VHDL, formats supporting register level description languages like RTL, and formats

supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, non-volatile storage media in various forms (e.g., optical, magnetic or semiconductor storage media) and carrier waves that may be used to transfer such formatted data and/or instructions through wireless, optical, or wired signaling media or any combination thereof. Examples of transfers of such formatted data and/or instructions by carrier waves include, but are not limited to, transfers (uploads, downloads, e-mail, etc.) over the Internet and/or other computer networks via one or more data transfer protocols (e.g., HTTP, FTP, SMTP, etc.).

When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, any of the specific numbers of bits, signal path widths, signaling or operating frequencies, component circuits or devices and the like may be different from those described above in alternative embodiments. Also, the interconnection between circuit elements or circuit blocks shown or described as multi-conductor signal links may alternatively be single-conductor signal links, and single conductor signal links may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments. Component circuitry within integrated circuit devices may be implemented using metal oxide semiconductor (MOS) technology, bipolar technology or any other technology in which logical and analog circuits may be implemented. With respect to terminology, a signal is said to be "asserted" when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be "deasserted" to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open drain or open collector condition). A signal driving circuit is said to "output" a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be "activated" when a signal is asserted on the signal line, and "deactivated" when the signal is deasserted. Additionally, the prefix symbol "/" attached to signal names indicates that the signal is an active low signal (i.e., the asserted state is a logic low state). A line over a signal name (e.g., '<signalname>') is also used to indicate an active low signal. The term "coupled" is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Integrated circuit device "programming" may include, for example and without limitation, loading a control value into a register or other storage circuit within the device in response to a host instruction and thus controlling an operational aspect of the device, establishing a device configuration or controlling an operational aspect of the device through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device. "AC-coupled" or "AC-coupling" refers to a capacitive or inductive interconnection between two nodes. An AC-coupled transmitter refers to a signal transmission circuit having a signal driver and an AC coupling between the signal driver and an output node of the AC-coupled transmitter. The term "exemplary" is used to express an example, not a preference or requirement.

While the invention has been described with reference to specific embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. For example, features or aspects of any of the embodiments may be applied, at least where practicable, in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. An integrated circuit IC, comprising:
interface circuitry to transfer data via a configurable-width data interface, the configurable-width data interface for coupling to:
a first independently accessible memory die of a set of memory dies connected using through-silicon-via (TSV) signal paths;
a second independently accessible memory die of the set of memory dies connected using the TSV signal paths;
wherein for a first mode of operation, the configurable-width data interface is of a first width; and
wherein for a second mode of operation, the configurable-width data interface is of a second width different than the first width.

2. The IC of claim **1**, wherein:
operation in the first mode of operation or the second mode of operation is based on a mode value.

3. The IC of claim **2**, wherein:
the mode value is retrieved from storage.

4. The IC according to claim **2**, wherein:
the mode value is provided to the IC from an external source.

5. The IC according to claim **1**, realized as a logic IC die.

6. The IC according to claim **5**, further comprising:
the set of memory dies disposed in a stacked relationship with the logic IC die.

7. The IC according to claim **1**, wherein:
the set of memory dies comprise dynamic random access memory (DRAM) memory dies.

8. The IC according to claim **1**, wherein:
the interface circuitry is to couple to one of the first independently accessible memory die or the second

independently accessible memory die, using the TSV signal paths, in response to a device-select signal.

9. An integrated circuit (IC) chip, comprising:

circuitry to transfer data via a configurable-width data interface between the IC chip and a stack of dynamic random access memory (DRAM) memory hips, the stack of DRAM memory chips interconnected using TSV signal paths;

wherein for a first mode of operation, the configurable-width data interface is of a first width; and

wherein for a second mode of operation, the configurable-width data interface is of a second width different than the first width.

10. The IC chip of claim **9**, wherein:

operation in the first mode of operation or the second mode of operation is based on a mode value.

11. The IC chip according to claim **10**, wherein:

the mode value is retrieved from storage.

12. The IC chip according to claim **10**, wherein:

the mode value is provided to the IC from an external source.

13. The IC chip according to claim **9**, realized as a logic IC chip.

14. The IC chip according to claim **13**, further comprising:

the stack of DRAM memory chips disposed in a stacked relationship with the IC chip.

15. The IC according to claim **9**, wherein:

the circuitry to transfer data is to couple to a first DRAM memory chip of the stack of DRAM memory chips, using the TSV signal paths, in response to a device-select signal.

16. A method of operation in an integrated circuit (IC) device, the method comprising:

configuring a data interface for coupling to

a first independently accessible memory die of a set of memory dies connected using through-silicon-via (TSV) signal paths;

a second independently accessible memory die of the set of memory dies connected using the TSV signal paths;

wherein for a first mode of operation, the configuring sets a data width for the data interface to a first width; and

wherein for the second mode of operation, the configuring sets the data width for the data interface to a second width that is different than the first width.

17. The method according to claim **16**, wherein:

the configuring sets the data width based on a mode value.

18. The method according to claim **17**, further comprising:

retrieving the mode value from storage.

19. The method according to claim **17**, further comprising:

receiving the mode value from an external source.

20. The method according to claim **16**, further comprising:

receiving a device-select signal; and

coupling the data interface to one of the first independently accessible memory die or the second independently accessible memory die in response to the device-select signal.

* * * * *

Exhibit 5

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(54) **METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING A POROUS SEMICONDUCTOR LAYER IN RF DEVICES**

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H01L 29/08	(2006.01)
H01L 23/66	(2006.01)
H03K 17/687	(2006.01)
H01L 21/762	(2006.01)

(52) **U.S. Cl.**

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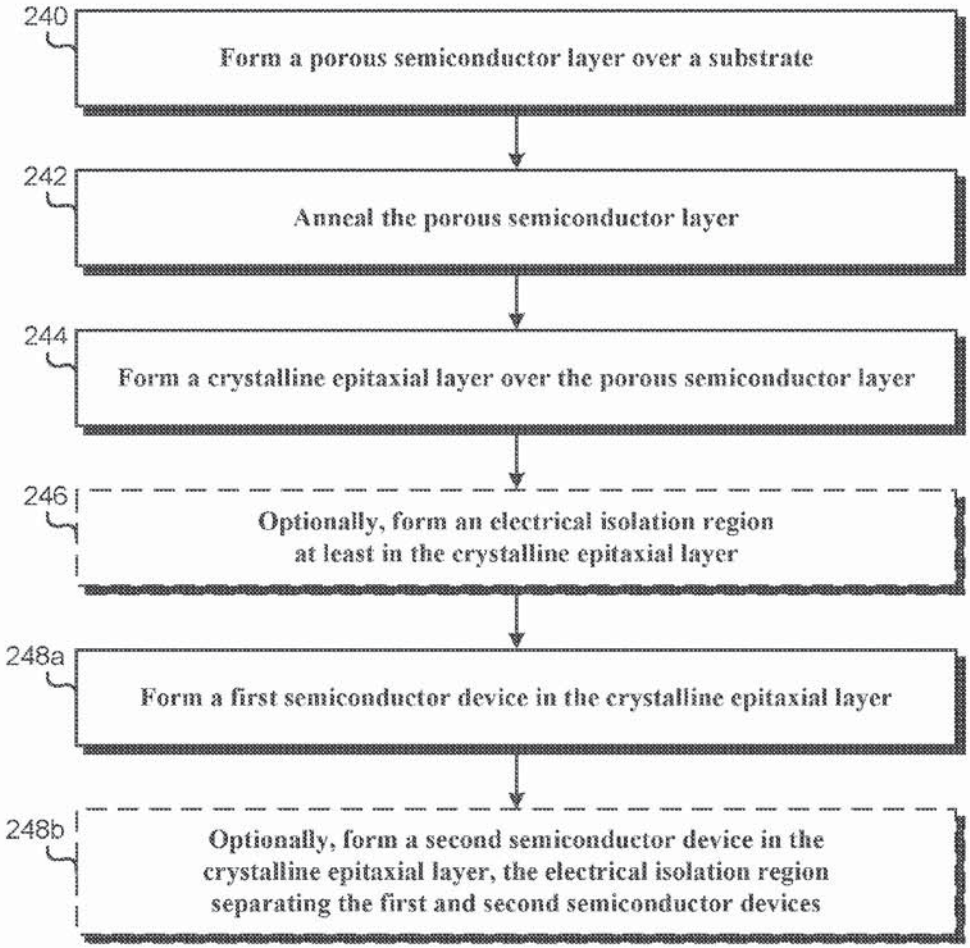
(57) **ABSTRACT**

A semiconductor structure includes a substrate having a first dielectric constant, a porous semiconductor layer situated over the substrate, and a crystalline epitaxial layer situated over the porous semiconductor layer. A first semiconductor device is situated in the crystalline epitaxial layer. The porous semiconductor layer has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor layer reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer, and an electrical isolation region separating the first and second semiconductor devices.



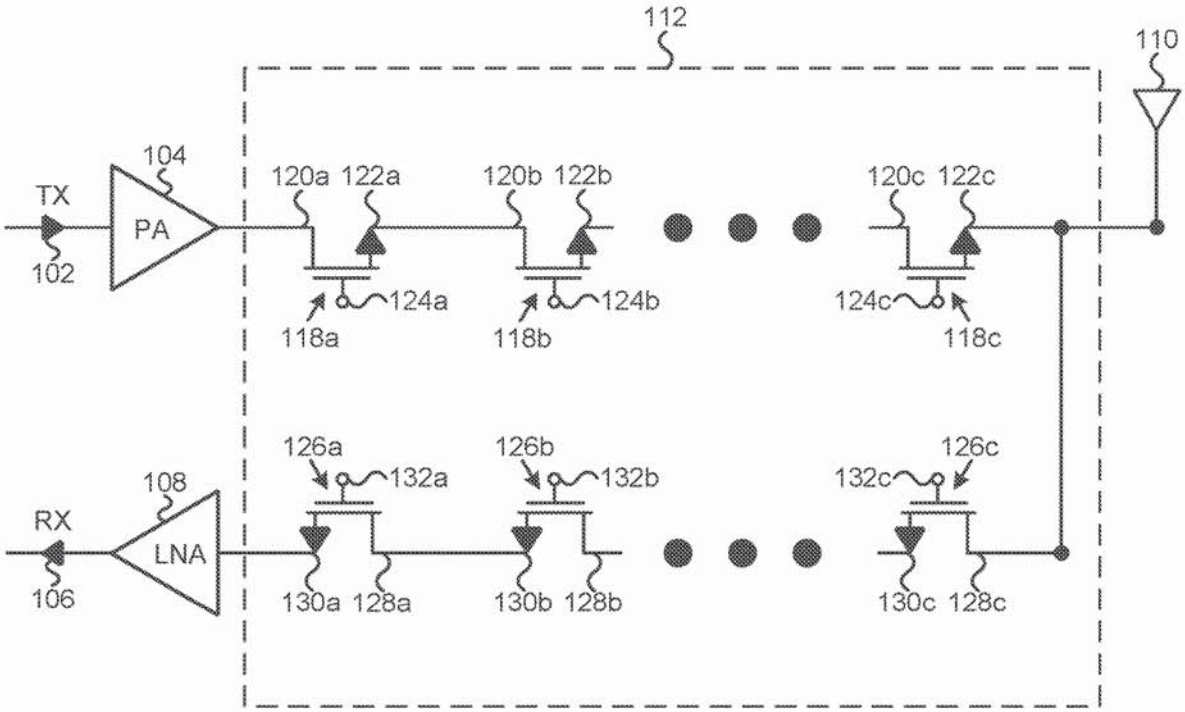

112
110
104
TX
PA
102
120a 122a
120b 122b
120c 122c
124a
124b
124c
118a
118b
118c
126a
126b
126c
132a
132b
132c
108
RX
LNA
106
130a 128a
130b 128b
130c 128c

FIG. 1

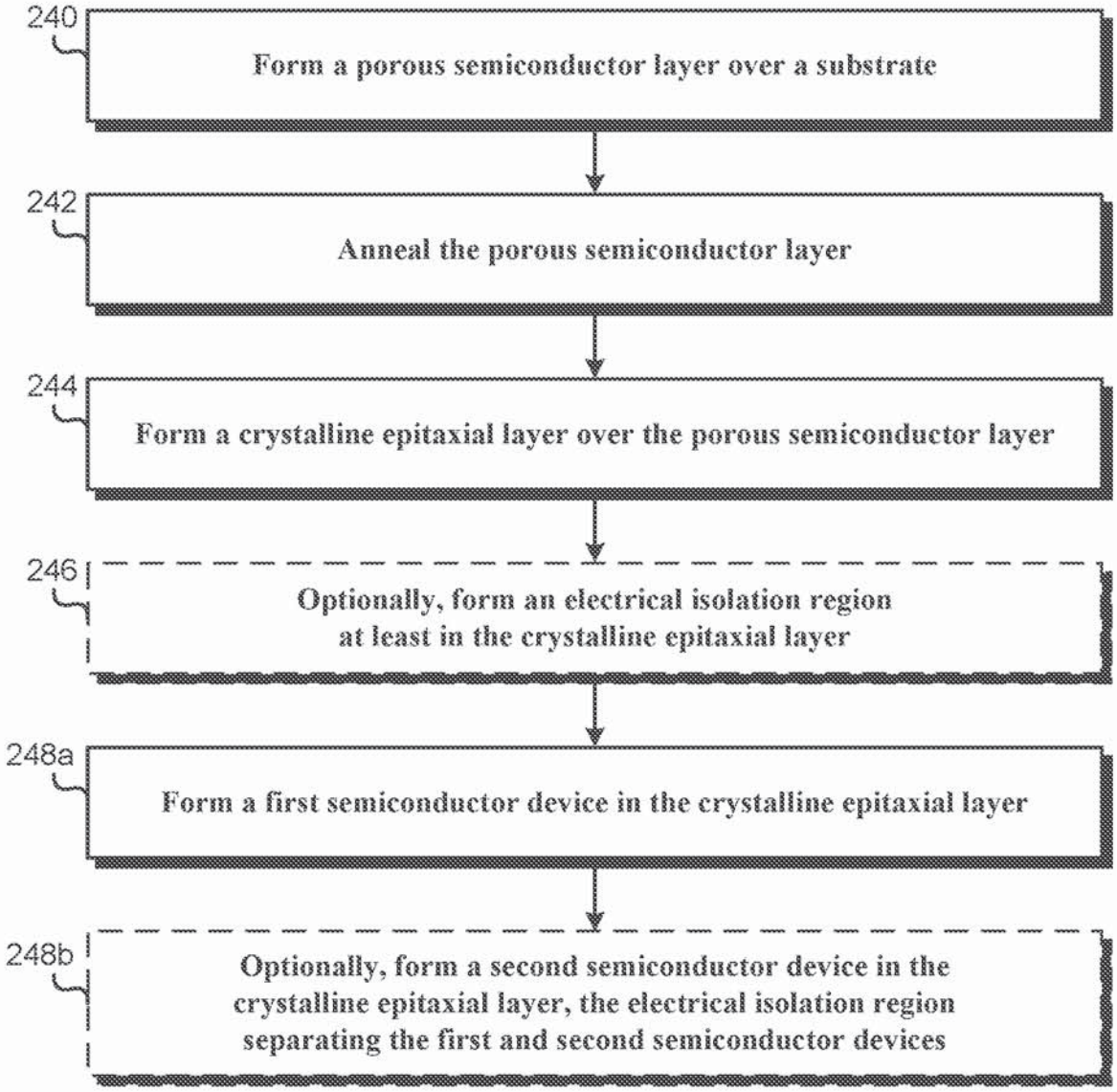

240
Form a porous semiconductor layer over a substrate
242
Anneal the porous semiconductor layer
244
Form a crystalline epitaxial layer over the porous semiconductor layer
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

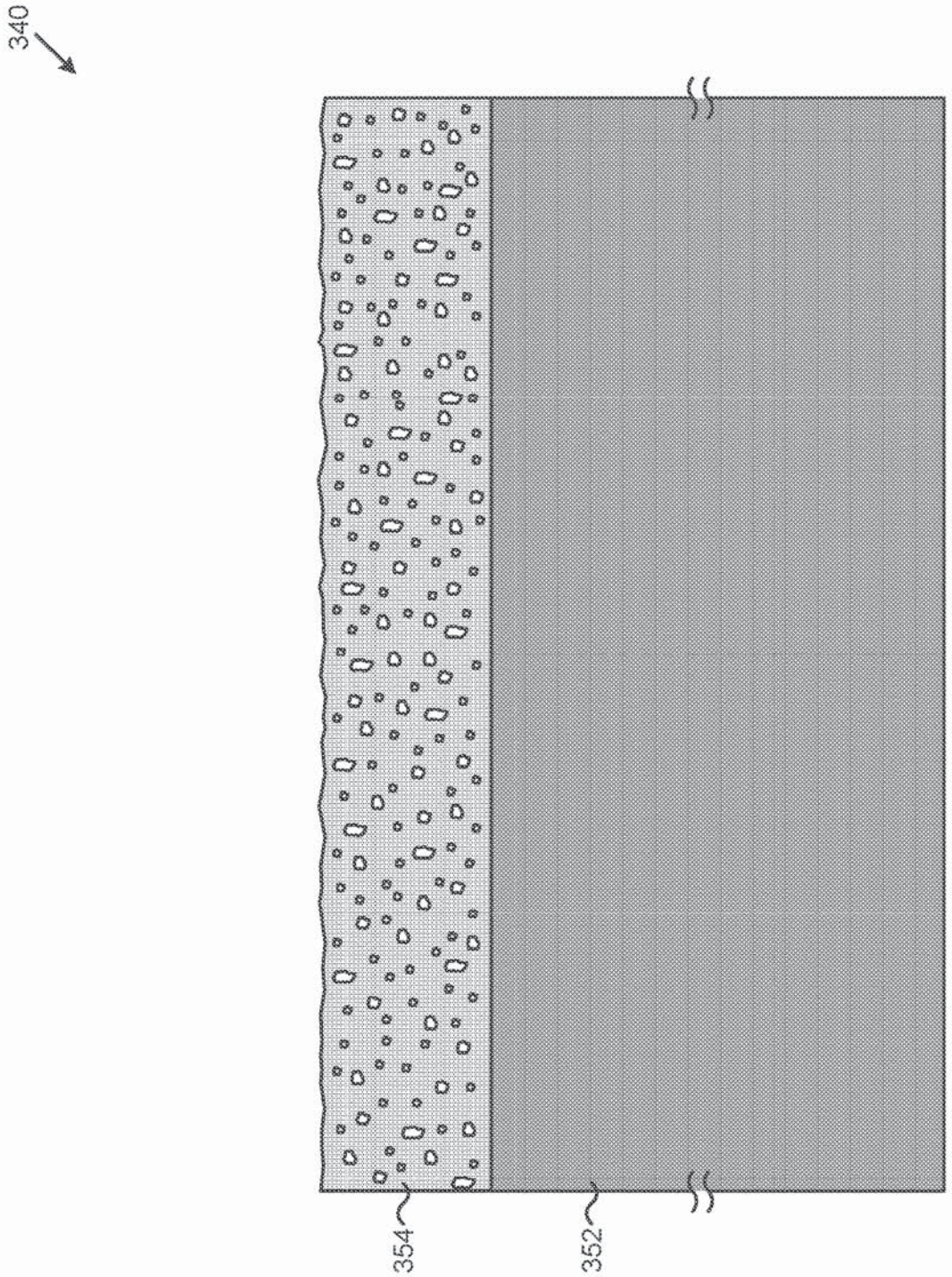


FIG. 3A

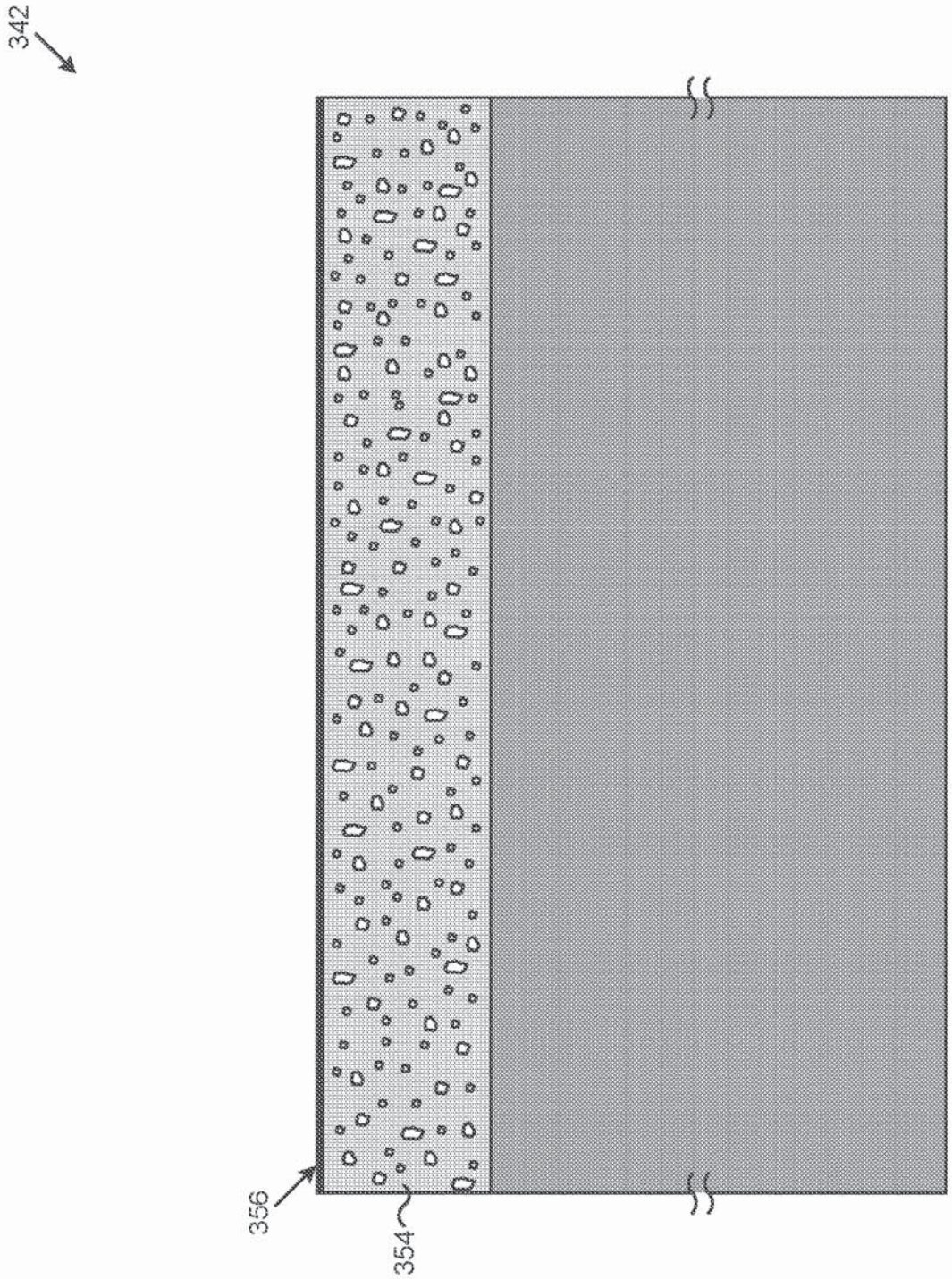


FIG. 3B

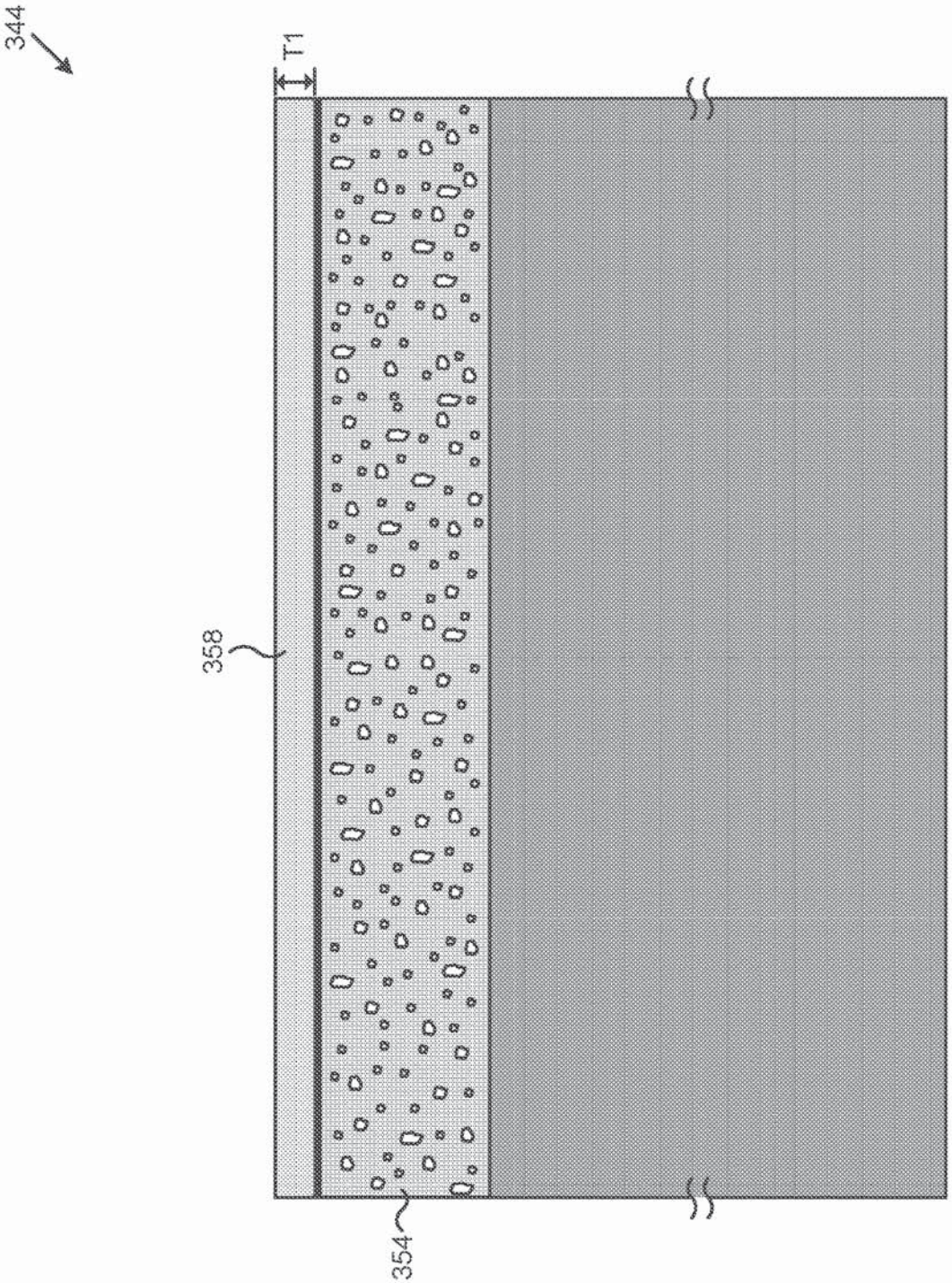


FIG. 3C

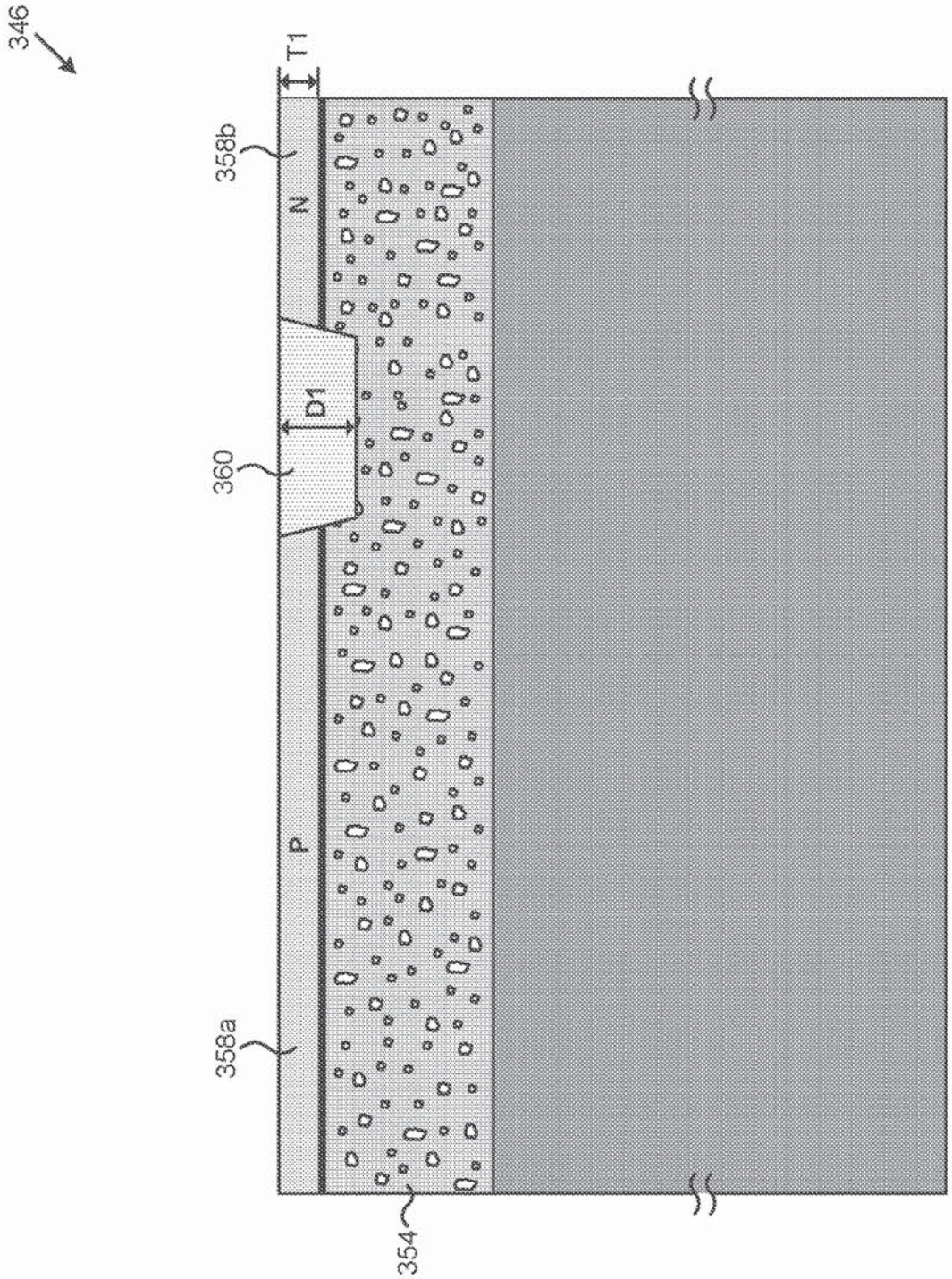


FIG. 3D

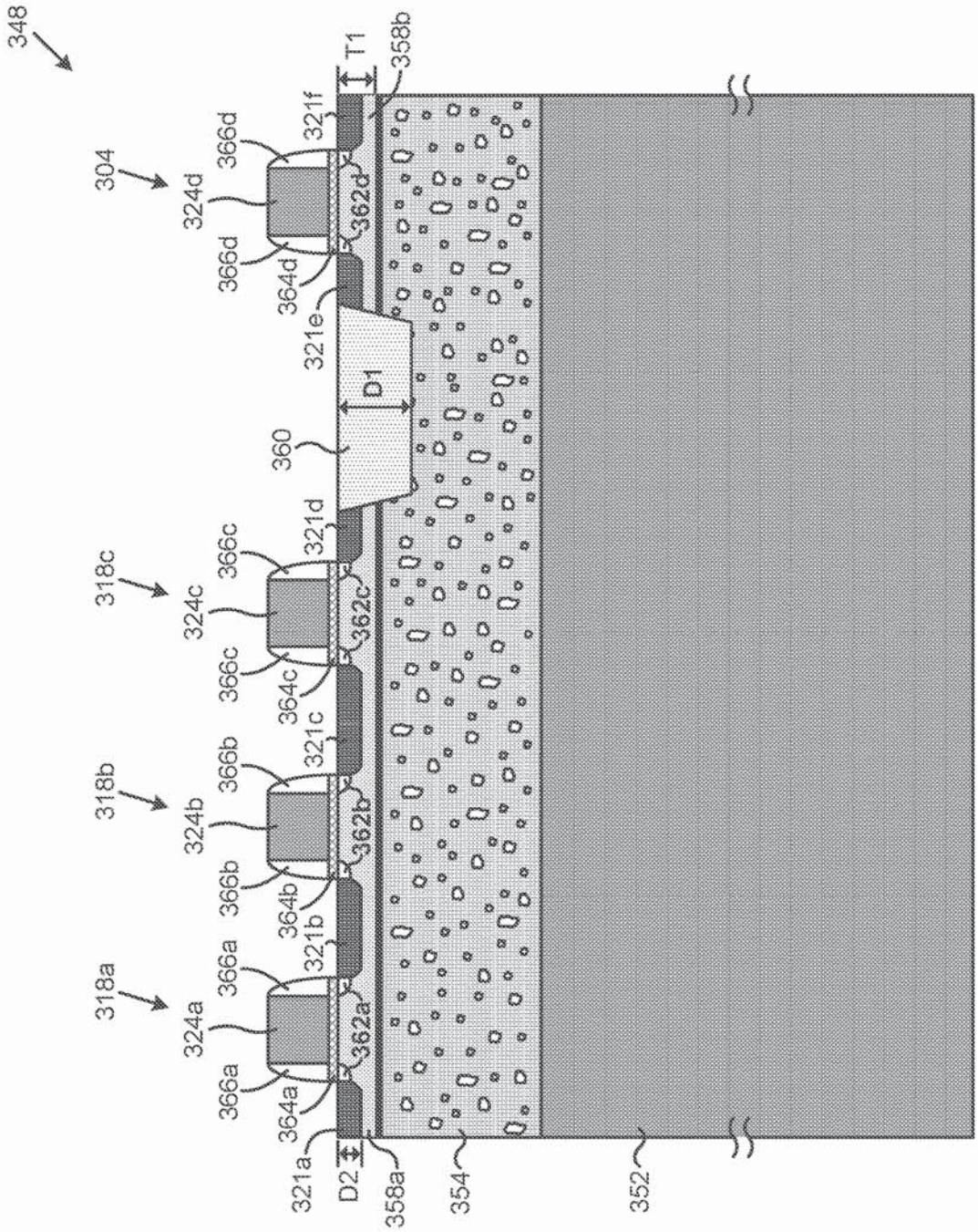

348
304
318a
318b
318c
324a
324b
324c
324d
366a
366b
366c
366d
364a
364b
364c
364d
362a
362b
362c
362d
321a
321b
321c
321d
321e
321f
D2
D1
T1
360
358a
358b
354
352

FIG. 3E

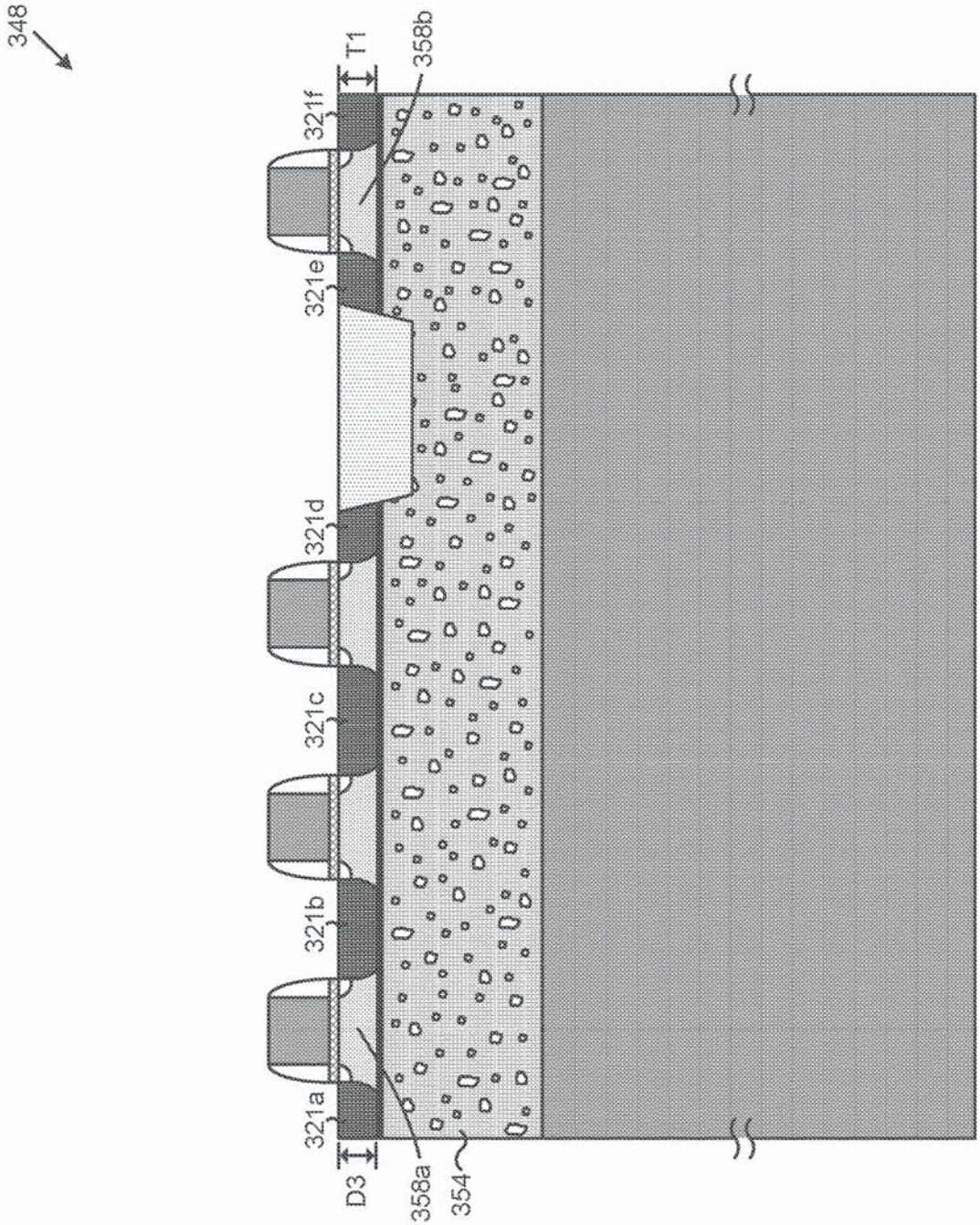


FIG. 3F

METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING A POROUS SEMICONDUCTOR LAYER IN RF DEVICES

BACKGROUND

[0001] Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

[0002] As known in the art, a handle wafer functioning as a. substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

[0003] Thus, there is need in the art for efficiently and effectively fabricating RF devices with reduced signal leakage at low cost while overcoming the disadvantages and deficiencies of the previously known approaches.

SUMMARY

[0004] The present disclosure is directed to a semiconductor structure having porous semiconductor layer for RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims,

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

[0006] FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

[0007] FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

[0008] FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

[0009] FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

[0010] FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

[0011] FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

[0012] FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

[0013] The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

[0014] FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

[0015] RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

[0016] RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in Figure can be coupled between RF switch **112** and LNA **108**, Receive output **106** receives amplified RF signals from LNA **108**. In one implementation, receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

[0017] RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

[0018] The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor

126*b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

[0019] In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to INA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

[0020] In the present implementation, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FEB (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF state voltage handling capability of forty volts (40 V). In various implementations, RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

[0021] As described below, in conventional semiconductor structures, signals can leak from RF switch **112**, for example, to ground or to other devices. This signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency signals, such as RF signals. According to the present application, RF switch **112** can be utilized in a semiconductors structure that reduces signal leakage. It is noted that, although the present application focuses on RF signals, the signals pray have frequencies other than RF frequencies.

[0022] FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

[0023] Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

[0024] FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown FIG. **3**A, according to action **240**, semiconductor structure **340** including porous semiconductor layer **354** situated over substrate **352** is formed. In the present implementation, substrate **352** is a bulk silicon substrate. For example, substrate **352** can be a P-type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, substrate **352** may be any other type of substrate.

[0025] Porous semiconductor layer **354** situated over substrate **352** is a semiconductor layer having voids, or pores, therein, Within porous semiconductor layer **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous semiconductor layer **354** can be formed by using a top-down technique, where portions of substrate **352** are removed to generate pores. For example, porous semiconductor layer **354** can be formed by electrochemical etching using hydrofluoric acid (HF). Alternatively, porous semiconductor layer **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art. Porous semiconductor layer **354** can also be formed by using a bottom-up technique, where deposition results in a semiconductor layer having empty spaces. For example, porous semiconductor layer **354** can be formed by low-temperature high-density plasma (HDP) deposition. Alternatively, porous semiconductor layer **354** can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous semiconductor layer **354** is a porous silicon layer, and has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous semiconductor layer **354** may be any other type of porous semiconductor layer.

[0026] FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous semiconductor layer **354** is annealed. For example, porous semiconductor layer **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous semiconductor layer **354** into larger cavities, while closing and smoothing surface **356** of porous semiconductor layer **354**. The annealed porous semiconductor layer **354** serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

[0027] FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous semiconductor layer **354**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material situated over porous semiconductor layer **354**. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and has thickness T**1** from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

[0028] FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation region **360** is formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358** and into porous semiconductor layer **354**.

[0029] Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358** and into porous semiconductor layer **354**, then depositing an electrically insulating material. In the present implementation, electrical isolation region **360** is also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using chemical machine polishing (CMP). Electrical isolation on **360** can comprise, for example, silicon dioxide (SiO_2).

[0030] In the present implementation, depth D**1** of electrical isolation region **360** is greater than thickness T**1** of crystalline epitaxial layer **358**. Accordingly, electrical isolation region **360** separates crystalline epitaxial layer **358** of FIG. **3**C into two crystalline epitaxial layers **358***a* and **358***b*. In one implementation, depth D**1** of electrical isolation region **360** can be substantially equal to thickness T**1**. In another implementation, depth D**1** of electrical isolation region **360** can be less than thickness T**1**, such that electrical isolation region **360** extends into crystalline epitaxial layer **358** but not into porous semiconductor layer **354**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation region **360**.

[0031] Crystalline epitaxial layers **358***a* and **358***b* can also be implanted with a dopant. For example, crystalline epitaxial layers **358***a* and **358***b* can be implanted with boron or other appropriate P-type dopant. In another example, one or both of crystalline epitaxial layers **358***a* and **358***b* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a* **358***b* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a* and **358***b* are implanted with a dopant after forming electrical isolation region **360**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation region **360**. In this implementation, electrical isolation region **360** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

[0032] As described below, electrical isolation region **360** reduces signal interference across crystalline epitaxial layers **358***a* and **358***b*. Electrical isolation region **360** is considered optional in that semiconductor structures according to the present application can be formed without electrical isolation region **360**.

[0033] FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. **3**E, semiconductor devices **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, semiconductor device **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates semiconductor device **304** from semiconductor devices **318***a*, **318***b*, and **318***c*.

[0034] In the present implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors. Semiconductor devices **318***a*, **318***b*, and **318***c* in FIG. **3**E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Semiconductor device **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Semiconductor device **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Semiconductor device **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

[0035] In the present implementation, semiconductor device **304** is also a transistor. Semiconductor device **304** in FIG. **3**E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Semiconductor device **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*. In one implementation, semiconductor device **304** can be utilized as part of a logic circuit. Semiconductor device **304** is considered optional in that semiconductor structures according to the present application can be formed without semiconductor device **304**.

[0036] Gates **324***a*, **324***b*, **324***e*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

[0037] In the present implementation, depth D**2** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T**1** of crystalline epitaxial

layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous semiconductor layer **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* and/or gates **324***a*, **324***b*, and **324***c*. In various implementations, semiconductor structure **348** can include more or fewer semiconductor devices in crystalline epitaxial layer **358***a*. In various implementations, crystalline epitaxial layers **358***a* and **358***b* can include diodes, or types of semiconductor devices instead of or in addition to transistors.

[0038] Because semiconductor structure **348** includes porous semiconductor layer **354** (for example, a porous silicon layer), semiconductor structure **348** reduces signal leakage (for example, RF signal leakage) from semiconductor devices **318***a*, **318***b*, **318***c*, and **304** to ground. Further, porous semiconductor layer **354** (for example, a porous silicon layer) reduces signal interference (for example, RF signal interference) between the different devices built in crystalline epitaxial layers **358***a* and **358***b*. Pores in porous semiconductor layer **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. **3**E, porous semiconductor layer **354** has a dielectric constant substantially less than the dielectric constant of substrate **352**. For example, when substrate **352** is a bulk silicon substrate having a dielectric constant of approximately 11.7, porous semiconductor layer **354** has a dielectric constant significantly less than 11.7. In particular, porous semiconductor layer **354** can have a dielectric constant from approximately 2.0 to approximately 4.0. The improved RF isolation that results from the low dielectric constant is especially advantageous for RF switching applications as it reduces signal distortion (i.e. improves linearity). It also results in a more uniform voltage distribution across the OFF state FET stack, increasing its power handling capability.

[0039] In semiconductor structure **348** in FIG. **3**E, utilizing porous semiconductor layer **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and substrate **352**. Accordingly, RF signals are less likely to leak from semiconductor devices **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to substrate **352**. For example, in one implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*, while the RF signals would have been subject to adverse impact of parasitic capacitances with substrate **352** if porous semiconductor layer **354** were not utilized. In other words, the RF signals could easily leak from semiconductor devices **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous semiconductor layer **354**, could. also result in a higher insertion loss.

[0040] Because semiconductor structure **348** includes porous semiconductor layer **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces signal interference from semiconductor devices **318***a*, **318***b*, **318***c* to semiconductor device **304**, and vice versa. If porous semiconductor layer **354** and electrical isolation region **360** were not utilized, signals (for example RF signals) from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or substrate **352**, and interfere with semiconductor devices **318***a*, **318***b*, **318***c* and generate additional undesirable noise in semiconductor devices **318***a*, **318***b*, **318***c*. Where semiconductor device **304** is a transistor utilized in PA **104** (shown in FIG. **1**), these consequences could be amplified. Together, the low dielectric constant of porous semiconductor layer **354** and electrical insulation of electrical isolation region **360** reduce signal leakage and interference through crystalline epitaxial layers **358***a* and **358***b* and/or substrate **352**. The leakage and interference are especially reduced where depth D**1** of electrical isolation region **360** is equal to or greater than thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*.

[0041] Semiconductor structure **348** in FIG. **3**E can achieve this reduced signal leakage without using costly materials for substrate **352**, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above porous semiconductor layer **354** (for example, a porous silicon layer) can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous semiconductor layer **354** (for example, a porous silicon layer) can be situated over bulk semiconductor substrate **352** (for example, a bulk silicon substrate), and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous semiconductor layer **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which semiconductor devices **318***a*, **318***b*, **318***c*, and **304** are formed. Further, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of semiconductor devices **318***a*, **318***b*, and **318***c* by reducing junction capacitances.

[0042] FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to cone implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D**3** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are in contact with porous semiconductor layer **354**. Compared to semi-

conductor structure **348** of FIG. **3**E, deeper source/drain junctions **321***e* and **321***f* in semiconductor structure **348** of FIG. **3**F improve performance of semiconductor device **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

[0043] From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

1-13. (canceled)

14. A method comprising:

forming a crystalline epitaxial layer over a porous semiconductor layer, said porous semiconductor layer being situated over a substrate;

forming a first semiconductor device in said crystalline epitaxial layer;

said substrate having a first dielectric constant, and said porous semiconductor layer having a. second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device.

15. The method of claim **14**, further comprising annealing said porous semiconductor layer prior to said forming said crystalline epitaxial layer.

16. The method of claim **14**, further comprising forming an electrical isolation region at least in said crystalline epitaxial layer.

17. The method of claim **16**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said crystalline epitaxial layer.

18. The method of claim **16**, further comprising forming a second semiconductor device in said crystalline epitaxial layer, wherein said electrical isolation region separates said first and second semiconductor devices.

19. The method of claim **14**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

20. The method of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

21. The method of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor layer.

22. A method comprising:

forming at least one crystalline epitaxial layer over a porous silicon layer in a semiconductor structure;

forming first and second transistors and an electrical isolation region separating said first and second transistors in said at least one crystalline epitaxial layer.

23. The method of claim **22**, further comprising forming said porous silicon layer over a bulk silicon substrate prior to said forming said at least one crystalline epitaxial layer.

24. The method of claim **22**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

25. The method of claim **22**, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon layer.

26. The method of claim **22**, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon layer.

27. A method comprising:

forming a porous semiconductor layer over a substrate, said porous semiconductor layer having a higher resistivity than said substrate;

forming at least one crystalline epitaxial layer over said porous semiconductor layer;

forming a first semiconductor device in said at least one crystalline epitaxial layer.

28. The method of claim **27**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material.

29. The method of claim **27**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a second semiconductor material.

30. The method of claim **27**, further comprising forming a second semiconductor device and an electrical isolation region separating said first and second semiconductor devices in said at least one crystalline epitaxial layer.

31. The method of claim **30**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

32. The method of claim **27**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

33. The method of claim **32**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

* * * * *

Exhibit 6

[Provisionally Filed Under Seal in its Entirety]

Exhibit 7

[Provisionally Filed Under Seal in its Entirety]

Exhibit 8

[Provisionally Filed Under Seal in its Entirety]

Exhibit 9

[Provisionally Filed Under Seal in its Entirety]

Exhibit 10

[Provisionally Filed Under Seal in its Entirety]

Exhibit 11

[Provisionally Filed Under Seal in its Entirety]